A reduced-code method for integral nonlinearity testing in DACs

A reduced-code method for Integral Nonlinearity testing in DACs

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Abstract

This paper proposes an innovative method for Integral Nonlinearity (INL) testing, that allows to measure the voltage corresponding only to a subset of all the codes of Digital-to-Analog Converters (DAC), shortening the duration of static characterization. The method operates, in fact, a pseudo-random selection of DAC codes to be tested but, through Compressed Sensing, it is able to recover the INL value for all the codes. The proposed method is experimentally evaluated on two DACs with different architectures and thus with different trends of the INL curve. In the performed tests, the recovered curve results very close to the INL curve obtained by the standard approach, while allowing a considerable time saving.

Keywords: Digital-to-Analog Converters, Nonlinearity Testing, Integral Nonlinearity, Static Testing, Compressed Sensing

1. Introduction

Data converter testing, referred to the set of techniques adopted to test Digital-to-Analog Converters (DAC) as well as Analog-to-Digital Converters (ADC), can be executed by following guidelines specified in proper standards [1, 2]. The standards distinguish between static and dynamic tests. Static tests are

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commonly used to determine parameters related to the transfer function of the DAC, such as Integral Nonlinearity (INL) and Differential Nonlinearity. Dynamic tests are instead used to provide parameters defined in the frequency domain, such as Spurious Free Dynamic Range or Signal-to-Noise-and-Distortion Ratio.

Long test times are required to evaluate data converters, especially in static testing. Static testing duration is, in fact, related to the huge number of output voltage values to be measured, each corresponding to a DAC code, and thus to the converter resolution. More specifically, completely testing an N-bit data converter means analyzing 2^N codes. Therefore, the test duration increases with the resolution. Besides, the measurement of each voltage value is typically performed through precision multimeters, that use long integration times to get the desired accuracy. Lastly, the test duration has a direct impact on the production costs of converters.

In some cases, knowing the DAC architecture can help to reduce the number of the employed codes, by exploiting the INL symmetry about the midpoint of the transfer function. In fact, in binary weighted DACs, the superposition principle is frequently observed. According to the superposition principle, the linearity error of a code equals the sum of the linearity errors of each bit in that code, due to lack of interaction among bits. If superposition holds, an N-bit DAC can be tested by measuring just the voltage values corresponding to the binary codes containing a single 1 and 0 in the remaining digits, as well as the immediately previous codes, to look at the bit transitions. Additionally, the voltage values corresponding to the first and the last code must be measured. Namely, INL can be evaluated from $2N$ overall DAC codes [3].

Unfortunately, architectures under test are usually unknown and, moreover, superposition does not hold in DACs that are fully decoded, segmented or Delta-Sigma and, at times, binary weighted [3]. In these cases, the voltage values must be necessarily characterized in correspondence to any of the codes. A possible solution to reduce static testing duration in such DAC architectures consists in saving time for the single measurement by means of built-in self-test schemes [4–

6]. In particular, a built-in self-test scheme for DAC static testing is suggested in [7] with a low resolution onboard digitizer, in place of a highly accurate voltmeter. Moreover, in [7] INL is modeled, known the architecture under test, as sum of three errors, associated with as many bit segments of the input code, through an algorithm that also compensates for digitizer nonlinearity. Since the INL model consists of the three contributions, the number of quantities to be estimated is reduced. Worth noting is that, despite the working principle of the algorithm is independent from the DAC architecture under test, knowing *a priori* the architecture is once again essential to segment the input code. Anyway, built-in self-test is inapplicable to commercial off-the-shelf DAC architectures.

This paper presents an innovative test method based on *Compressed Sensing* (CS) [8] that reduces the remarkable duration of DAC static characterization. The DAC output is characterized on a reduced number of input codes, nevertheless, the INL curve is recovered on all the codes. It should be noted that the reduced-code method proposed in this paper is more general than the code reduction mentioned in [3], as it is not based on the superposition principle. Even more significantly, no knowledge of DAC architectures is needed before testing, differently from the methods described in [3, 7]. The proposed method relies on the assumption that in a transform domain (such as the Fourier Transform domain) INL is *sparse*, i.e. expressible through a few significant coefficients, by neglecting all the others. As already observed in [9] for ADCs, INL does not have a broad frequency content, but it is concentrated in specific frequency ranges. By means of this observation, INL is modeled in [9] by a high-frequency component plus a low frequency component, which is approximated with a polynomial law. In this paper, such observation is applied to DACs, that, in general, are characterized by similar INL trends. Moreover, the proposed method does not require to know in advance the positions of INL frequency components, as it automatically estimates the components with higher magnitude.

The proposed reduced-code method has been preliminarily introduced in [10], where a first evaluation was carried out through numerical simulations. In this paper, a more detailed description of the method is provided. Furthermore, an

experimental assessment on two DACs is presented, reporting the accuracy of the method versus the all-codes standard approach and the effective advantage in terms of measurement time. The structure of the paper is organized as reported below. Section 2 describes the reduced-code method for INL testing in DACs. In Section 3, the proposed method is experimentally validated, while in Section 4 its performance is analyzed in comparison to the standard approach. Conclusions and future developments are drawn in Section 5.

2. The proposed method

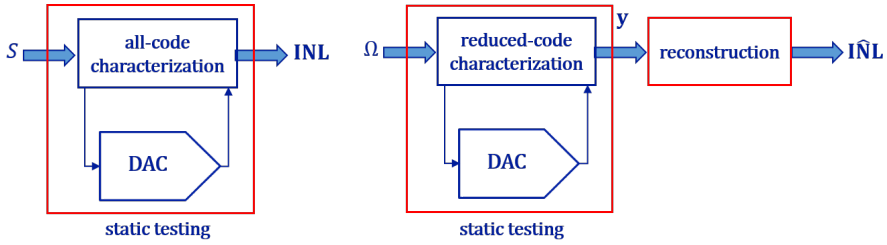
DAC static testing is basically implemented through a setup where various digital codes are generated and applied as input, while the output voltage is measured by an instrument, such as a voltmeter [1, 3]. In some cases, the measurement process is automated and controlled by a computer, especially if testing is carried out by manufacturers [3]. Nevertheless, in many cases, code switching is still performed manually.

As established by the IEEE Standard 1658 [1], for a complete assessment of the INL curve in DACs, static testing is based on considering all the input codes. The standard approach for INL testing in DACs, depicted in Fig. 1a, is briefly recalled. In an N-bit DAC the output voltage is characterized on the set S of all the $K = 2^N$ input codes:

$$S = \{k\}_{k=0}^{K-1}, \tag{1}$$

where k is the value of the binary coded input [1]. Thus, static testing is implemented by proceeding one by one from the first code up to the code that corresponds to full scale. The input codes are usually applied in increasing order. However, if desired, the input codes can be applied in decreasing order, too. In general terms, the measured output voltage $U(k)$, corresponding to the input code k, deviates of a small quantity from the ideal output voltage, corresponding to the same input code. Such difference is the linearity error in voltage:

$$\varepsilon(k) = U(k) - Qk - U(0), \tag{2}$$



(a) standard approach (b) proposed method

Figure 1: Block scheme of (a) all-code method and (b) reduced-code method for static testing in DACs.

with Q the voltage of the Least Significant Bit (LSB), i.e. the ideal code bin width, defined as [1]:

$$Q = \frac{U(K-1) - U(0)}{K-1}, \tag{3}$$

where the numerator is the full scale range of the DAC output. The INL value, corresponding to the input code k, represents the linearity error in LSB:

$$INL(k) = \frac{\varepsilon(k)}{Q}. \tag{4}$$

The standard approach requires that, once the output voltage $U(k)$ is measured, (2) and (4) are computed to get the INL value for each DAC code k, providing the whole INL curve:

$$\mathbf{INL} = \frac{1}{Q}\begin{bmatrix} \varepsilon(0) \\ \varepsilon(1) \\ \vdots \\ \varepsilon(K-1) \end{bmatrix}. \tag{5}$$

The method proposed in this paper needs to measure the output voltages corresponding only to a subset of DAC codes and, later, reconstructs the INL curve through the CS theory [8]. Essentially, a first phase retraces the standard approach, but employing less input codes to save time, while a second phase recovers entirely the INL curve. These two main phases are detailed below.

In the first phase, a reduced number of input codes $M < K$ is selected for the DAC static characterization. Specifically, the first code and the last code

are always selected from the 2^N original codes: $k_0 = 0$ and $k_{M-1} = K - 1$. The choice of the remaining $M - 2$ codes is pseudo-random: they are picked without repetitions on the basis of a Gaussian distribution from the whole set of codes, excluding the first one and the last one. As depicted by the block diagram of Fig. 1b, the DAC output voltage is then characterized on the subset of the selected input codes:

$$\Omega = \{k_m\}_{m=0}^{M-1}. \tag{6}$$

The INL value, corresponding to the input code $k_m \in \Omega$, is evaluated by following the (4). The relation between the whole INL curve and the INL evaluated only on the selected codes can be modeled by a linear transformation taking into account the selection process. Specifically, the INL evaluated on the M selected codes is expressed as:

$$\mathbf{y} = \mathbf{\Phi}\ \mathbf{INL}, \tag{7}$$

where $\mathbf{\Phi}$ is the *sensing matrix*, namely an $M \times K$ rectangular matrix, which models the selection process as:

$$\mathbf{\Phi} = [\mathbf{I}]_{\Omega,:}, \tag{8}$$

with $[\cdot]_{\Omega,:}$ a restriction operator which selects the rows of the identity matrix $\mathbf{I}$ according to the indices m of the codes contained in Ω. The identity matrix $\mathbf{I}$ has size K, i.e. it is a $K \times K$ matrix with ones on the main diagonal and zeros elsewhere. Each row of the matrix $\mathbf{I}$ identifies a value of the vector $\mathbf{INL}$. In other words, the selection process reduces the rows of the identity matrix $\mathbf{I}$ by a factor K/M, named Reduction Factor (RF). Therefore, the advantage of the proposed method consists precisely in reducing the duration of static testing by directly reducing the values of the INL curve to be estimated and, correspondingly, the input codes employed to characterize the values of the DAC output voltage. If the INL curve of a 16-bit DAC has to be evaluated, for instance, the standard approach requires that $K = 65536$ codes are employed for characterization. Instead, by considering the proposed method with $RF = 4$, the number of codes to be employed is drastically limited to $M = 16384$.

In the second phase, the whole INL curve is reconstructed starting from the vector $\mathbf{y}$. As above mentioned, the method relies on the assumption that a few significant coefficients can represent the whole INL curve in a specific transform domain, while the other ones can be neglected. Under such sparsity assumption, the INL curve can be expressed as:

$$\mathbf{INL} = \mathbf{\Psi c}, \tag{9}$$

where $\mathbf{\Psi}$ is a $K \times K$ transform matrix, from the transform domain to the code domain, and $\mathbf{c}$ is a sparse coefficient vector. The matrix $\mathbf{\Psi}$ must be properly chosen as *sparsity basis*, to represent the transform domain where the INL curve of the device under test expresses more its sparsity. In this paper, the choice for the sparsity basis is carried out through experimental analysis, observing the results obtained by several transforms. From (7) and (9), the following expression holds:

$$\mathbf{y} = \mathbf{\Phi \Psi c}. \tag{10}$$

By exploiting the CS theory, the coefficient vector $\mathbf{c}$ can be recovered from the reduced INL vector (7) and the sensing matrix (8). Thus, among all the possible vectors satisfying the system (10), the coefficient vector $\mathbf{c}$ with the smallest number of non-null elements is found [8]:

$$\hat{\mathbf{c}} = \arg\min_{\mathbf{c}} \|\mathbf{c}\|_0 \quad : \quad \mathbf{y} = \mathbf{\Phi \Psi c}, \tag{11}$$

with the symbol $\|\cdot\|_0$ denoting the ℓ_0-norm that counts the non-null elements of the vector. In [8] it is demonstrated that the problem (11), which is computationally intensive, can be rewritten as an ℓ_1-norm problem:

$$\hat{\mathbf{c}} = \arg\min_{\mathbf{c}} \|\mathbf{c}\|_1 \quad : \quad \|\mathbf{y} - \mathbf{\Phi \Psi c}\|_2 \leq \delta, \tag{12}$$

where δ is a positive threshold that takes into account INL variability. Once the coefficient vector is estimated, the INL curve can be reconstructed as:

$$\hat{\mathbf{INL}} = \mathbf{\Psi}\hat{\mathbf{c}}. \tag{13}$$

In summary, the presented method can be outlined in five steps: (i) pseudo-random selection of a subset of DAC codes from the all-code set; (ii) measurement of the output values corresponding to the selected codes; (iii) evaluation of INL from the measured values; (iv) recovery of the INL coefficients in the transform domain; (v) reconstruction of the entire INL curve.

3. Experimental validation of the proposed method

The proposed method for static INL testing, described in previous Section 2, was validated and compared to the standard approach. As already mentioned in Section 1, in [10] the effectiveness of the method had been numerically investigated on a DAC behavioural model, available on the website of the manufacturer [11]. For this paper, the proposed method was experimentally implemented on two DACs having different architectures and thus different trends of the INL curve. First of all, a DAC with a binary weighted architecture was considered, as its working principle is based on the superposition law. Therefore, a 12-bit R-2R DAC integrated in an STMicroelectronics STM32H743ZI microcontroller was used for a first evaluation of the proposed method. Also a second DAC with an architecture where the superposition principle does not hold was considered. In particular, Delta-Sigma DACs are mentioned in [3] as one of the architectures where the code reduction based on the superposition principle cannot be applied. Thus, for a second evaluation of the proposed method, a Cirrus Logic WM8994 audio codec was selected, since its audio generation path includes a 16-bit Delta-Sigma DAC.

For both the architectures, the DAC output was acquired through the EVAL-AD717xSDZ evaluation board. The EVAL-AD717xSDZ evaluation board includes an AD7177 Delta-Sigma ADC with 24-bit resolution. A preliminary assessment of the AD7177 ADC was carried out by means of the test setup shown in Fig. 2. DC voltage levels, spanning the ADC range with a step of 1 mV, were generated by a Fluke 5500A calibrator and given both to the AD7177 ADC and to a Fluke 8508 digital multimeter. The ADC test was repeated for in-

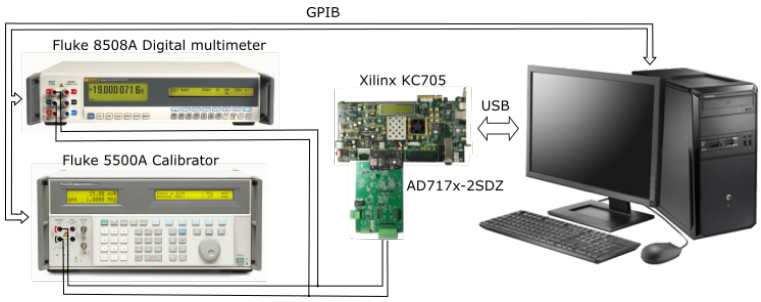
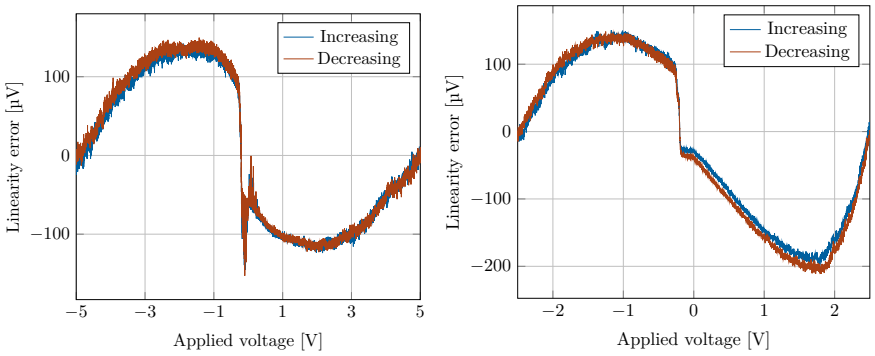


Figure 2: Test setup employed for the calibration of the AD7177 ADC.

creasing and decreasing voltage levels in the two considered ranges of the ADC: [-2.5, 2.5] V and [-5, 5] V. For each voltage value provided by the calibrator, 1000 ADC samples were collected and their average was considered. For both the considered ADC ranges, the transfer function was measured and the linearity error was obtained by subtracting the value measured by the digital multimeter from the value measured by the ADC and then eliminating offset and gain errors, according to the terminal-based definition, i.e. such that the linearity error is null in the first and the last code. The results are reported in Fig. 3 for both the considered ranges, versus the applied voltage levels, measured by means of the Fluke 8508A multimeter. The linearity error shows a maximum absolute value in the order of 100 µV and a very little difference between the values obtained in increasing and decreasing directions.

For each of the two considered DACs, the INL curve was firstly obtained through the standard approach, for comparison with the INL curve reconstructed by the proposed method. In both the cases, the INL curve was then compensated by removing the portion of the ADC linearity error falling in the range of the DAC. Finally, the proposed method was applied, by randomly selecting the M codes to be used, according to a given reduction factor RF. Then, starting from the voltage values corresponding only to the selected codes, the vector $\mathbf{y}$ was built and the whole INL was reconstructed, by solving (12) and evaluating (13). In particular, the minimization problem (12) was solved in MATLAB environment by means of the Orthogonal Matching Pursuit (OMP)



(a) Range [−5, 5] V

(b) Range [−2.5, 2.5] V

Figure 3: Linearity error measured for the AD7177 ADC on the two ranges: (a) [-5, 5] V and (b) [-2.5, 2.5] V, with increasing (in blue) and decreasing (in red) voltage levels.

algorithm [12]. In order to apply the proposed method, it is necessary to select a proper sparsity basis $\mathbf{\Psi}$ to be used to model the INL curve. In this paper, several Fourier-related transforms are investigated for the sparsity basis: Discrete Fourier Transform (DFT), Discrete Cosine Transform (DCT), Discrete Hartley Transform (DHT) and Discrete Walsh-Hadamard Transform (DWHT), successfully used for the characterization of data converters [13]. The results of this section refer to the use of the DFT. In the following subsections, the details of the tests for each considered DAC are provided.

3.1. Test implementation on the DAC in STM32H743ZI microcontroller

3.1.1. Test bench

The test bench used in the first evaluation phase, shown in Fig. 4, employs a NUCLEO-H743ZI board, embedding the STM32H743ZI microcontroller, a computer and an Analog Devices EVAL-AD717x-2SDZ evaluation board, adopted to measure the DAC output. Code generation and signal acquisition are driven by the computer running a MATLAB program. An Agilent 6032A is employed to provide a DC power supply to the NUCLEO-H743ZI board. The AD7177 ADC is configured with a range of [-5, 5] V.

The computer sends the code to be tested to the microcontroller of the

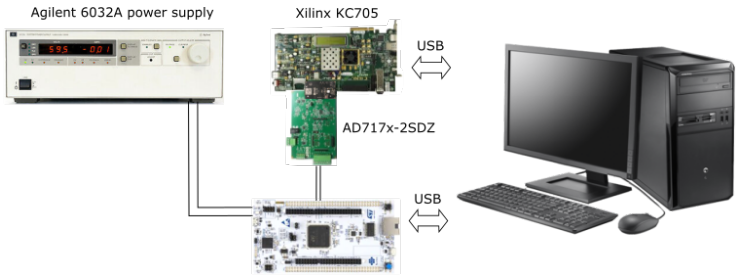


Figure 4: Test bench employed to implement the proposed method on the DAC of NUCLEO-H743ZI board.

NUCLEO-H743ZI board through the Universal Serial Bus (USB) interface. The microcontroller writes then the received code onto the register of the DAC, that modifies the corresponding output voltage. The EVAL-AD717x-2SDZ evaluation board, connected to the DAC output pin, measures 1000 times the voltage value generated by the DAC. The acquired samples are transferred by an Analog Devices SDPI-I-FMC evaluation board and a Xilinx Kintex-7 FPGA KC705 evaluation board, connected to the computer via USB interface. Finally, the MATLAB program computes the average of the 1000 voltage values. In order to reduce the contribution of noise and other random effects in the first evaluation phase, the characterization of the DAC output value was repeated 10 times. Then, the average of the 10 acquisitions was computed.

3.1.2. The INL curves

Fig. 5 shows in blue the INL curve obtained on all the codes. The INL curve was compensated by removing the portion of the ADC linearity error falling in the DAC range [0, 3.3] V. The INL curve obtained after the compensation is shown in red in Fig. 5.

For the OMP implementation, it is necessary to specify the number of iterations of the algorithm. The number of iterations determines the number of nonzero elements in the estimated vector $\hat{\mathbf{c}}$, since the OMP resolves a nonzero element at each iteration. Thus, the number of iterations influences the accuracy of the reconstructed INL. However, increasing the number of iterations

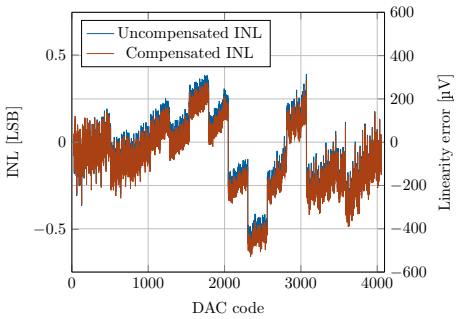


Figure 5: INL of the DAC integrated in the STM32H743ZI microcontroller, obtained on all codes, before (blue) and after (red) the compensation of the ADC INL.

increases also the algorithm complexity. In this paper, the suggested procedure for determining the number of iterations to be used is to observe the Root Mean Square (RMS) difference between two increasing values of the number of iterations, such to check whether such difference is still relevant for the required test accuracy. In Fig. 6, the RMS difference between each number of iteration and the previous one is shown for $RF = 10$ and a number of iterations in the range [10, 300], with a step of 10. The RMS difference presents a higher slope at the beginning, which means a highest relative improvement of the estimation for low numbers of iterations. Then, the slope decreases. The selected value should be chosen in the region where the slope is lower. For the tests, a value of 200 was selected, marked with the red circle in Fig. 6.

Fig. 7 shows the results obtained with the application of the proposed method, for $RF = 10$ and 200 iterations of the OMP. In particular, in Fig. 7a the INL curve obtained by the proposed method (in red) is overlapped to the reference one, obtained on all the codes. The graph shows a good overlapping between the curves. The good performance of the reconstruction can be observed also by the low voltage difference between the two curves, in Fig. 7b, which is in the order of hundreds of µV. The reconstructed curve exhibits a little higher variability within some code ranges. Fig. 8a and Fig. 8b show two enlargements of Fig. 7a, respectively on code ranges $[2200 - 2500]$ and $[2400 - 2700]$, where the deviation of the reconstructed INL curve from the original INL curve can

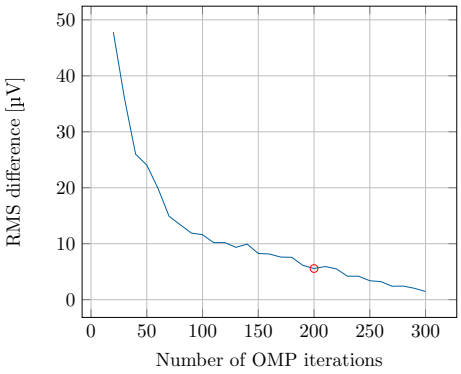
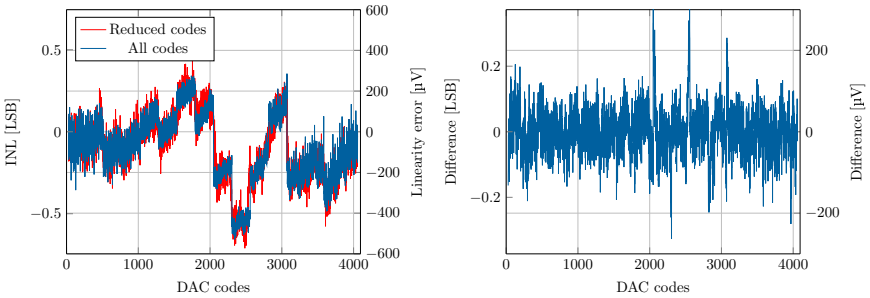


Figure 6: RMS difference of the value obtained for a given number of iteration and the previous one for the DAC integrated in the STM32H732ZI microcontroller. The selected value should lie in the region with the lower slope.



(a) Reconstructed and all codes INLs

(b) Difference between the reconstructed and the all codes INL

Figure 7: Results obtained for the DAC integrated in STM32H743ZI microcontroller: (a) the all codes INL (in blue) and the INL with the application of the proposed method (in red), for a RF of 10; (b) difference between the two curves.

be appreciated. This higher difference is mainly due to the reduced number of DFT coefficients estimated in the reconstructed curve, leading to a smoothing of the INL steps.

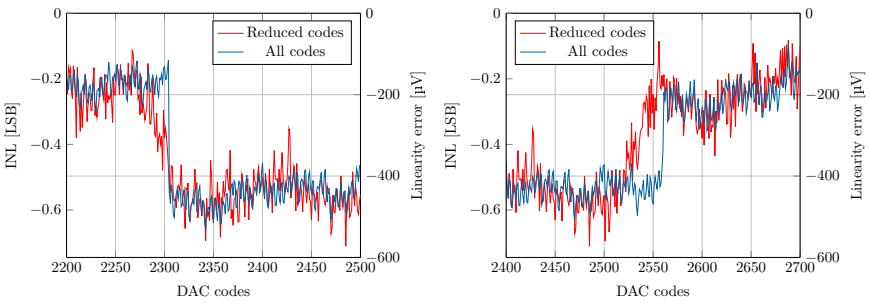


Figure 8: INL enlargement on code ranges (a) $[2200 - 2500]$ and (b) $[2400 - 2700]$.

3.2. Test implementation on the DAC of Cirrus Logic WM8994 audio codec

3.2.1. Test bench

The test bench employed for the second evaluation phase is depicted in Fig. 9. It consists of an STMicroelectronics 32F476DISCOVERY board, that embeds the Cirrus logic WM8994 audio codec and an STM32F756NG microcontroller, an Analog Devices EVAL-AD717x-2SDZ board and a computer. The 32F476DISCOVERY board is connected to the computer by USB interface and to the EVAL-AD717x-2SDZ board through Serial Peripheral Interface (SPI). Moreover, the audio output of the 32F476DISCOVERY board is connected to the analog input of the EVAL-AD717x-2SDZ board (in blue in Fig. 9). The AD7177 ADC is configured with a range of [-2.5 2.5] V.

A command from the computer instructs the STM32F746NG microcontroller to start the test. Once the test starts, the microcontroller writes a constant code (beginning from the lowest code) to the Serial Audio Interface, connecting the microcontroller to the WM8994 integrated on the 32F476DISCOVERY board. The WM8994 codec changes accordingly the output value. Then, the microcontroller reads the value acquired by the AD7177 ADC through the SPI and updates the DAC input code.

3.2.2. The INL curves

Similarly to the procedure followed for the other DAC, the INL curve obtained by the standard approach was firstly determined and compensated by removing the portion of the ADC linearity error. In Fig. 10 the all codes INL curve is shown before (in blue) and after the compensation (in red).

In order to determine the number of iterations to be used, the OMP algorithm was executed for different numbers of iterations in the range [10, 300], with a step of 10. The RMS difference of the reconstructed INL curve obtained with the current and the previous number was evaluated. The results referring to $RF = 10$ are shown in Fig. 11. The trend of the curve is similar to the case of the other DAC, with a steeper slope for a low number of iterations. Then the slope decreases as the number of iterations increases. The number of iterations to be used should be selected in the region with the lower slope. As in the previous case, a number of iterations of 200 was selected (marked by the red circle in the figure).

The results obtained by applying the proposed method on the second DAC are shown in Fig. 12. In Fig.12a the all code INL curve and the curve recon-

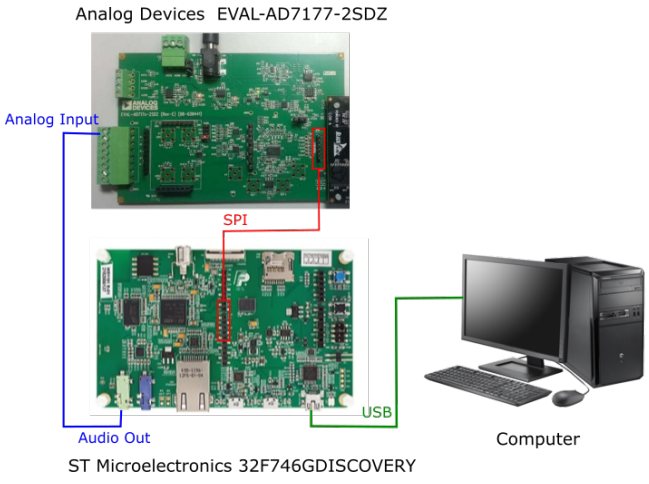


Figure 9: Test bench employed to implement the proposed method on the DAC of 32F746GDISCOVERY board.

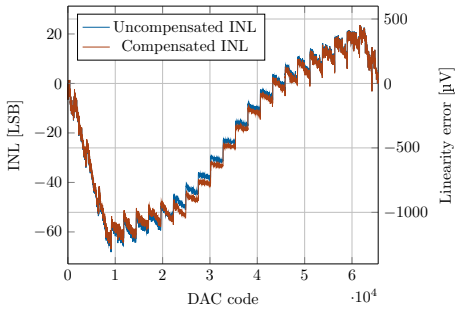


Figure 10: INL of the DAC of the WM8994 codec, obtained on all codes, before (blue) and after (red) the compensation of the ADC INL.

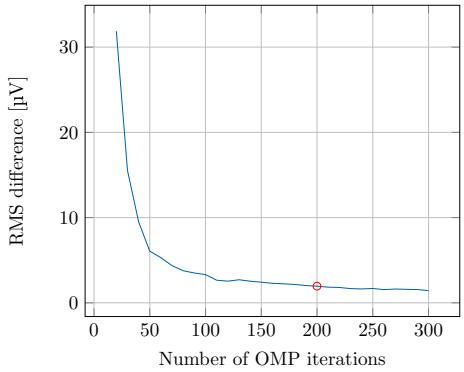
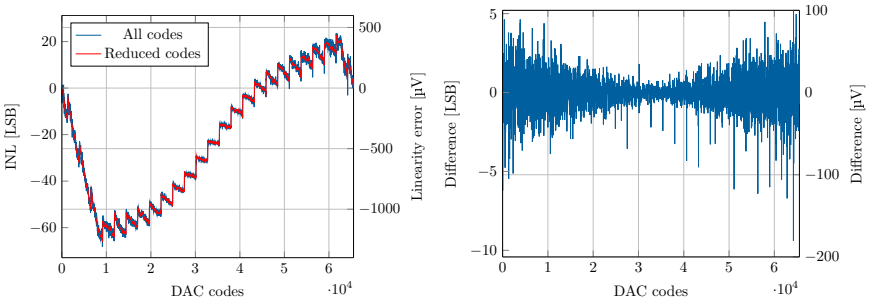


Figure 11: RMS difference of the value obtained for a given number of iteration and the previous one for the DAC of the WM8994 codec. The selected value should lie in the region with the lower slope.

structed by the proposed method with $RF = 10$ are shown in blue and in red, respectively. The figure shows a good overlapping of the curves. Fig. 12b reports the difference of the two curves which is in the order of 100 µV.

The good agreement of the curves can be better observed in the two enlargements of Fig. 12a, reported in Fig. 13, within the code ranges [29000 - 34000] and [50000 - 55000]. It can be observed that the curve reconstructed by the proposed method well follows the steps of the reference curve. In this case, the reconstruction operates a denoising of the original waveform, by removing the high-frequency variability, because of the reduced number of non-zero elements of the coefficient vector in the Fourier domain.



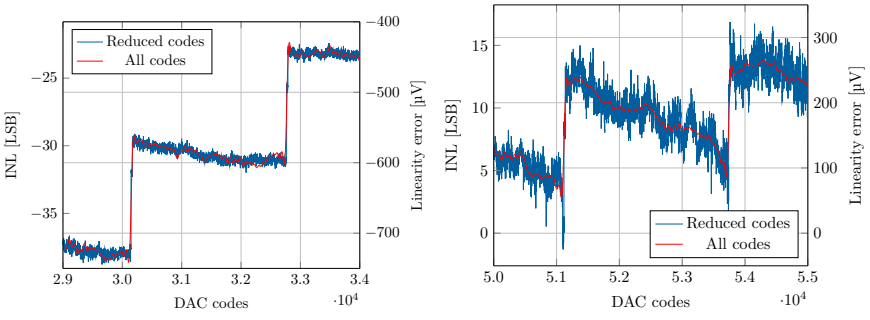
(a) Reconstructed and all codes INLs

(b) Difference between the reconstructed and the all codes INL

Figure 12: Results obtained for the DAC in the WM8994 codec: (a) the all codes INL (in blue) and the INL with the application of the proposed method (in red), for a RF of 10; (b) difference between the two curves.

3.3. Time analysis

On completion of this Section, in order to evaluate the actual time reduction in the proposed method, a comparison with the duration of the standard approach is carried out. Generally speaking, the longer the measurement time of a single voltage value is, the greater the time advantage in the proposed method is. Besides, the time saving is higher when increasing the resolution of the DAC under test.



(a) (b)

Figure 13: INL enlargement on code ranges (a) $[29000 - 34000]$ and (b) $[50000 - 55000]$.

Table 1: Testing times in the two methods for static INL.

DAC board	single measurement	standard approach	proposed method		
		characterization	RF	characterization	reconstruction
NUCLEO-H743ZI	1.6 s	1 hour 49 minutes	7	16 minutes	0.3 s
			10	11 minutes	0.1 s
32F746GDISCOVERY	0.2 s	3 hours 38 minutes	7	31 minutes	126.8 s
			10	22 minutes	27.6 s

For illustrative purposes, an analysis of times needed during the two experimental implementations of the method is reported in Tab. 1, depending on $RF = \{7, 10\}$. The experimental test implementation to measure a voltage value required about 1.6 s for the DAC of the NUCLEO-H743ZI board, since the acquired voltage was, indeed, the average of 1000 values. For the DAC of the 32F746GDISCOVERY board, where single acquisitions were performed, 0.2 s were required. Obviously, the measurement of the DAC output voltage was repeated for each of the $2^{12} = 4096$ and $2^{16} = 65536$ input codes, respectively. Thus, the INL testing based on standard approach entailed an overall duration approximately of 1 hour 49 minutes in the first case and 3 hours 38 minutes in the second case. Instead, by applying the proposed method with $RF = 10$, the duration of static characterization would be limited to 11 minutes for the first DAC and 22 minutes for the second DAC. When the proposed method is applied, also the time for INL reconstruction must be included in overall test duration. Considering that, as shown in Tab. 1, few minutes at most are required by the minimization algorithm for INL reconstruction, the duration of testing procedure is considerably lowered anyway.

4. Performance evaluation

In this Section, the performance of the proposed method is evaluated by comparing the reconstructed vector $\hat{\mathbf{INL}}$ (13) to the original vector **INL** (5). The figure of merit adopted for the comparison is the Root Mean Square Error

(*RMSE*):

$$RMSE = (\mathbf{INL} - \hat{\mathbf{INL}})_{rms} = \sqrt{\frac{1}{K}\sum_{k=0}^{K-1}[INL(k) - \hat{INL}(k)]^2}. \quad (14)$$

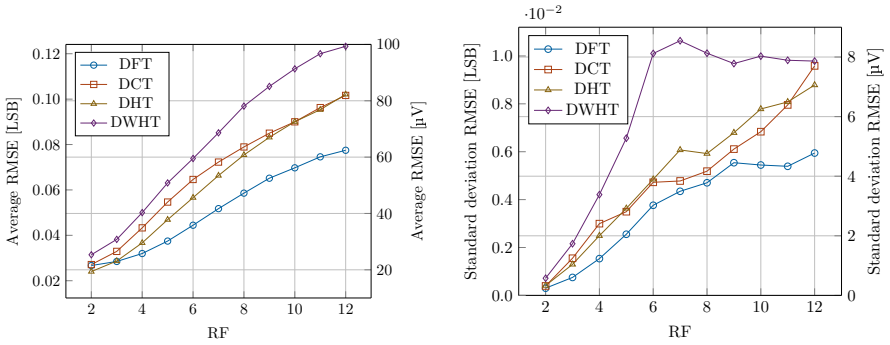
4.1. Analysis strategy

The analysis was performed on the output values obtained by the two considered DACs, as described in Sections 3.1.1 and 3.2.1. The *RMSE* evaluation was carried out in MATLAB environment. The investigation was executed on increasing *RF* values, with the number of OMP iterations set to 200. Furthermore, the inverses of the following matrices were considered: (i) DFT matrix, (ii) DCT matrix, (iii) DHT matrix, (iv) DWHT matrix.

Since the process to select the codes in the sensing matrix (8) is random, the reconstructed vector $\hat{\mathbf{INL}}$ was evaluated for 200 random trials and the *RMSE* was computed at each trial. Thus, the average of the obtained *RMSE* values was computed. In order to take into account the repeatability of the proposed method depending on the selected input codes, the standard deviation of the 200 *RMSE* values was computed as well.

4.2. Results

The averaged $RMSE$ values related to the analysis of the first considered DAC are shown in Fig. 14a depending on $RF = \{2, 3, \ldots, 12\}$. As expected, the average values increase with RF. Very small *RMSE* values are actually obtained up to $RF = 12$. The standard deviation is represented in Fig. 14b. It increases with RF by an order of magnitude smaller than the average, so *RMSE* in the 200 random trials does not significantly deviate from the averaged values. Among all the considered Fourier-related transforms, the inverse DFT matrix generally exhibits the lowest *RMSE*, both as average and standard deviation. The results of DCT and DHT are almost comparable and slightly higher than the results obtained through DFT. Finally, the DWHT matrix displays the lowest performance.

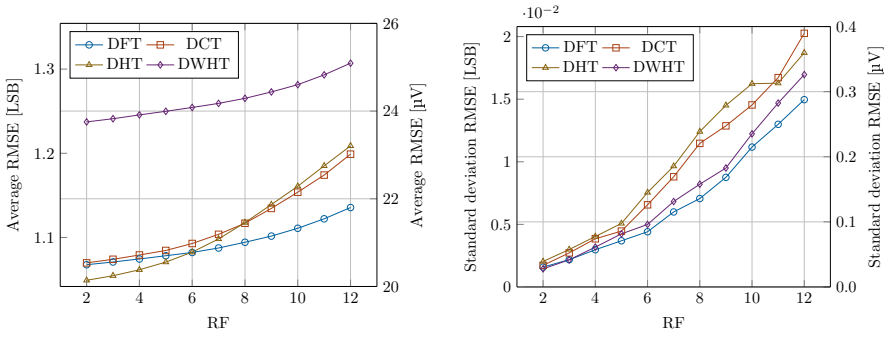


(a) average (b) standard deviation

Figure 14: (a) Average and (b) standard deviation of $RMSE$ values versus RF obtained for the DAC of the NUCLEO-H743ZI board.

The averages and the standard deviations for the analysis of the second architecture are shown in Fig. 15a and Fig. 15b depending on $RF = \{2, 3, \ldots, 12\}$. Both the values increase with RF. Worth noting is that in this case the standard deviation turns out even smaller by two order of magnitude than the average. Once again, the inverse DFT matrix generally shows the best performance and the $RMSE$ values resulting from DCT and DHT are comparable. Instead, differently from the previous analysis, the averaged $RMSE$ values obtained through DWHT differ significantly from all the other averaged $RMSE$ values.

It should be emphasized that, on the basis of the obtained results, the proposed reduced-code method proves to be very performing. Such results are particularly encouraging to reduce the duration of static characterization. Obviously, as visible by Tab. 1 of Subsection 3.3, more the input codes are reduced, greater saving time is. On the other hand, $RMSE$ grows with RF increase. As a consequence, the right compromise between time and performing results should be chosen to apply the proposed method in static characterization. A good trade-off can be represented, as instance, by the value $RF = 7$, where the $RMSE$ values committed on average with the DFT matrix are just 0.05 LSB and 1.09 LSB, respectively for the first and the second DAC, corresponding to 41.7 µV and 20.9 µV.



(a) average (b) standard deviation

Figure 15: (a) Average and (b) standard deviation of *RMSE* values versus *RF* obtained for the DAC of the 32F746GDISCOVERY board.

5. Conclusion

In this paper a method for static nonlinearity testing in DACs based on reduced codes has been proposed. In a first phase, the method retraces the standard approach, after the input codes employed to characterize the DAC output are pseudo-randomly selected. In a second phase, the INL curve is completely recovered on all the codes, by means of a minimization algorithm.

The proposed method was experimentally tested on two DACs. In both cases, the reconstructed INL curve reveals very close to the curve obtained by the standard approach, but it is determined with a considerable saving of time. Several Fourier-related transforms were investigated for the sparsity basis, showing the best performance through the inverse DFT matrix. The performance analysis was carried out also on increasing *RF* values, confirming low reconstruction errors for a factor as high as 12. Indeed, more the input codes are reduced, greater the saving time and, simultaneously, the error are. Therefore, to apply the proposed method in static characterization, a compromise between time and performing results should be reached. For example, an $RF = 7$ is a good compromise for the experimental implementation on both the adopted test benches.

Future work will be extended to nonlinearity testing in ADCs. Firstly, non-idealities and noise affecting the process of static characterization will be numerically evaluated. Secondly, the method will be also experimentally implemented on several ADC architectures, by analyzing its actual impact on accuracy and duration for INL testing.

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