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Abstract: The purpose of the present research endeavor is to propose a novel control strategy for a DC-DC electrical converter realized as a switched circuit. The present endeavor is based on an early work by Leonard and Krishnaprasad where a prototypical DC-DC converter was modeled as a state space dynamical system and controlled by an open-loop strategy based on Lie group theory. In this work, we shall rather introduce a closed-loop control strategy based on maximum convergence rate, study some features of the novel method, and illustrate its behavior by numerical simulations. A numerical comparison of the two methods complements the paper. The numerical comparison shows how the proposed feedback control method outperforms the static one in terms of convergence rate and resiliency against parameters mismatch.

Keywords: DC-DC electrical converter; open-loop control; feedback control; switched electrical network

1. Introduction

Switched electrical networks are systems that consist of interconnected subsystems or components that can be controlled or switched on and off. Switched systems appear in a wide range of applications, including power systems, telecommunications, and transportation systems [1]. In power systems, for example, switched networks can be used to model the operation of power generators, transmission lines, and loads. In telecommunications, switched networks are used to model the routing of data packets through a network of routers and switches. In transportation systems, switched networks can be used to model the operation of traffic lights and other control systems. Further applications are found in mechanical engineering and computer science [2], as well as other areas such as robotics, biomedical engineering, and environmental engineering.

A prominent instance of a switched system is a DC-voltage to DC-voltage (DC-DC) converter. DC-DC converters turn out to be essential components in a wide range of electronic systems, and they play a crucial role in converting sourced DC voltages to desired levels that suit the needs of different devices. There exist several different types of DC-DC converters, each with their own advantages and disadvantages, and the appropriate type depends on the specific application requirements. High-frequency DC-DC converters offer the advantage of smaller and lighter components but also present additional challenges, which can be addressed through different constructive topologies and control techniques. Modeling and analyzing DC-DC converters are of prime importance for understanding their behavior and predicting their performance.

There exist several methods for analyzing and synthesizing switched systems, including traditional methods such as Lyapunov stability analysis and modern methods such as hybrid system theory and nonlinear system theory [3]. Stability analysis is an important aspect of switched systems, as it determines whether a system is able to maintain its equilibrium or desired behavior over time. Control design is another important aspect of switched systems, as it involves the design of controllers or algorithms that can be used



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Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). to steer the system towards a desired behavior. Switched systems with delays are also of particular interest, as some real-world systems exhibit non-negligible delays due to the inherent limitations of physical components or communication networks [4].

In the present paper, we shall take as a case study the prototypical model of a switched DC-DC converter studied in [5] and briefly revise its mathematical description as a first-order dynamical system (in three variables). In the first place, we shall revise some salient features of this electrical scheme that, being lossless, admits an invariant that shapes its state space to be a curved manifold. A lossless converter is one that presents no energy dissipation or, equivalently, a unitary conversion rate and represents henceforth an ideal system. Electrical energy conservation is an instance of symmetry, since state transition in such systems is modeled through mathematical operators that leave a quadratic form of the system's state unvaried.

We shall subsequently point out that the open-loop control strategy proposed in [5] is characterized by some advantages and some drawbacks that we propose to mitigate through a closed-loop control strategy that is much simpler to implement yet provides comparable performances. The design and implementation of the control algorithm makes explicit reference to manifold theory, a branch of mathematical analysis that, in the context of non-linear control, allows for dealing seamlessly with curved state spaces.

The present paper is organized as follows. Section 2 recalls the prototypical DC-DC converter examined by Leonard and Krishnaprasad in [5] along with its state space mathematical model and emphasizes some of its salient mathematical features. Section 3 summarizes a number of technical aspects related to the design of DC-DC converters. Section 4 reviews the Lie group-based control strategy deployed in [5] along with its salient features and drawbacks. Section 5 introduces a closed-loop control strategy to transfer the energy content from the input side of the converter to the output side based on maximum convergence rate. Section 6 illustrates the behavior of the introduced control strategy by a number of numerical tests, as well as a comparison of the introduced strategy with the original Leonard–Krishnaprasad method. Section 7 concludes the paper.

2. Electrical and Mathematical Model of a Prototypical DC-DC Converter

The present section summarizes the main features of DC-DC converters and illustrates the mathematical model of a prototypical converter.

2.1. Generality of DC-DC Converters

DC-DC converters are electronic circuits that convert direct current (DC) from one voltage level to another and constitute a viable counterpart to electrical transformers that may only be used in alternate current (AC) circuits. DC-DC converters are widely employed in a variety of applications, including power supplies for electronic devices, electric vehicles, and renewable energy systems [6–9]. There exist several types of DC-DC converters, including buck converters, boost converters, buck–boost converters, and Ćuk converters. Each type has its own advantages and disadvantages, and the appropriate type for a given application depends on the specific requirements and constraints.

Buck converters are used to step down the input voltage to a lower output voltage. They operate by switching the input voltage at a high frequency and using inductors and capacitors to filter the voltage ripple. The output voltage can be controlled by adjusting the duty cycle of the switching signal. Boost converters, on the other hand, are used to step up the input voltage to a higher output voltage.

Buck–boost converters can operate in either a buck mode or a boost mode, depending on the input and output voltage levels. They are often used in applications where the input voltage may be either higher or lower than the desired output voltage. Also, Ćuk converters are a hybrid of the buck and boost converters, and they can achieve a high conversion ratio, although their topology is generally more complex; a non-isolated Ćuk converter comprises two inductors, two capacitors, a switch and a diode. They are often used in high-power applications where a high conversion ratio is required. High-frequency DC-DC converters are those that operate at switching frequencies above a few hundred kilo-Hertz. They have the advantage of smaller and lighter components, but they also present the challenge of higher losses and electromagnetic interference (EMI) issues. Various topologies and control techniques have been developed to address these challenges and to enable the use of high-frequency DC-DC converters in a wide range of applications.

Modeling and analysis techniques for DC-DC converters are important for understanding their behavior and predicting their performance. Small-signal modeling and modal analysis are widely used approaches for this purpose. These methods involve linearizing the converter equations around the operating point and analyzing the resulting linear system to determine the dynamic response of the converter.

2.2. A Prototypical Converter Model and Its State Space Description

Direct current converters have been realized in various electrical configurations [10–12], which invariably contain an energy source (typically an electrical capacitor), an energy buffer (typically a capacitor), an energy-bridging element (typically an electrical inductor), and a switch that realizes a variable topology structure. Electronic switches in power applications are realized as (groups of) thyristors (for a review of high-power thyristors in power electronics applications, see, e.g., [13,14]), while MOSFET is the typical device in low-power applications.

As a prototypical model of a switched DC-DC converter, we adopted the circuital scheme studied in [5], as shown in Figure 1.



Figure 1. Prototypical circuital scheme of a DC-DC converter adapted from [5], where $C_1 > 0$, $C_2 > 0$, and $L_3 > 0$.

At the beginning of the energy transfer cycle, the capacitor C_1 is charged at a voltage $V_1(0)$, which constitutes the input to the converter, and the inductor current intensity $I_3(0) = 0$, while the capacitor C_2 contains no charges; hence, $V_2(0) = 0$. The control problem consists in transferring the electrical energy initially stored in C_1 to C_2 , through the inductor L_3 , by an appropriate sequence of commutations of the switch. In fact, the inductor serves as a temporary energy storage at every commutation.

By network analysis, it is found that the state space representation of the converter in Figure 1 is given by the following set of three differential equations:

$$\begin{cases} C_1 \frac{dV_1}{dt} = (1-u)I_3, \\ C_2 \frac{dV_2}{dt} = uI_3, \\ L_3 \frac{dI_3}{dt} = -(1-u)V_1 - uV_2, \end{cases}$$
(1)

where the variable $u \in \{0, 1\}$ constitutes the control input to the system and $t \in [0, t_f]$, where $t_f > 0$ denotes the total duration of a conversion cycle, namely, the total time allotted to the converter to transfer energy from the input capacitor to storage capacitor

and, with reference to Figure 1, an input value u = 1 means that the switch is in the right-hand position.

Notice that the circuit in Figure 1 is devoid of dissipative elements, which corresponds to considering ideal (lossless) components. In addition, the energy buffer capacitor C_2 is not connected to any load. In the considered idealized model drawn from [5], the capacitor C_1 is substantially discharged into the capacitor C_2 by using an inductor as a temporary energy storage element and a switch to connect these three elements so that the energy transfer takes place. In normal operations, an electrical load might be a low-power DC motor [15] or a low-power AC motor connected to the DC supply through an inverter [10].

In the present idealized context, the energy content of the circuit stays unvaried over time, as shown in the following result.

Theorem 1 (Energy conservation in the idealized DC-DC converter). *The total instantaneous electrical energy content of the circuit in Figure 1 is conserved over time (irrespective of the control input).*

Proof. The total instantaneous electrical energy content of the circuit in Figure 1 is defined as

$$E(V_1, V_2, I_3) := \frac{1}{2}C_1V_1^2 + \frac{1}{2}C_2V_2^2 + \frac{1}{2}L_3I_3^2.$$
(2)

It can be immediately verified that

$$\frac{\mathrm{d}E(V_1, V_2, I_3)}{\mathrm{d}t} = (1-u)V_1I_3 + uV_2I_3 - (1-u)I_3V_1 - uI_3V_2 = 0, \ \forall t \in [0, t_f].$$
(3)

Therefore, the energy content is conserved over time. \Box

The above theorem illustrates the existence of a symmetry in the system representing a lossless DC-DC energy converter.

At the end of the control cycle, whose duration is denoted as t_f , it is expected that $V_1(t_f) = 0$ and $I_3(t_f) = 0$. Since the circuit is lossless, the following energy conservation property holds:

$$\frac{1}{2}C_1V_1^2(0) = \frac{1}{2}C_2V_2^2(t_f).$$
(4)

Therefore, the output voltage of the converter will be

$$V_2(t_f) = \pm \sqrt{\frac{C_1}{C_2}} V_1(0).$$
(5)

We therefore see that the circuital model under analysis may realize a buck–boost converter depending on the ratio C_1/C_2 between the capacitance values.

Since the electrical circuit is lossless, the state space of the circuit is not the entire flat space \mathbb{R}^3 but a curved space. To make such a conclusion more evident, it is convenient to introduce the new state variables

$$x^{(1)} := \sqrt{C_1} V_1, \ x^{(2)} := \sqrt{C_2} V_2, \ x^{(3)} := \sqrt{L_3} I_3 \tag{6}$$

as well as the state vector $x := \begin{pmatrix} x^{(1)} & x^{(2)} & x^{(3)} \end{pmatrix}^{\top}$. Notice that the states $x^{(1)}$ and $x^{(2)}$ are measured in VF^{1/2}, while the state $x^{(3)}$ is measured in AH^{1/2}. (V is the International System unit for Volt, F for Farad, and H for Henry.) The mathematical model (1) may then be recast as

$$\dot{x}(t) = (A + Bu(t))x(t), \ x(0) = (\sqrt{2E_0} \ 0 \ 0)^{\top},$$
(7)

where $E_0 > 0$ denotes the energy content of the source (in joules) and, following [5], we have defined the constant matrices

$$A := \begin{pmatrix} 0 & 0 & \omega_1 \\ 0 & 0 & 0 \\ -\omega_1 & 0 & 0 \end{pmatrix}, B := \begin{pmatrix} 0 & 0 & -\omega_1 \\ 0 & 0 & \omega_2 \\ \omega_1 & -\omega_2 & 0 \end{pmatrix}$$
(8)

with $\omega_1 := 1/\sqrt{C_1L_3}$ and $\omega_2 := 1/\sqrt{C_2L_3}$. In terms of the new state variable vector, the conservation of energy reads

$$E(x^{(1)}, x^{(2)}, x^{(3)}) = \frac{1}{2}x^{\top}x = E_0,$$
(9)

which makes it apparent how the state space of the converter, in the normalized variables, is a three-dimensional sphere of radius $\sqrt{2E_0}$.

From a dynamical system perspective, energy conservation stems from the algebraic structure of the system (7), in which it can be immediately recognized that both matrices A and B are skew-symmetric, namely $A^{\top} = -A$ and $B^{\top} = -B$. As a consequence, it holds that $\dot{E} = x^{\top} \dot{x} = x^{\top} A x + (x^{\top} B x) u = 0$, irrespective of the values taken by the control input. In other terms, as the state x evolves, the point of coordinates x traces a curve laying on a spherical shell described by the equation $x^{\top} x = 2E_0$. In manifold calculus, such a surface is denoted as $\sqrt{2E_0}S^2$, which represents a 3D sphere of radius $\sqrt{2E_0}$.

Generalizing from [5], we fix the target state to be $\bar{x}(t_f) = \begin{pmatrix} 0 & -\sqrt{2E_0} & 0 \end{pmatrix}^{\top}$. The objective of control design is to steer the state of the system from the initial state x(0) to the desired final state $\bar{x}(t_f)$ under the constraint imposed by the dynamics (7), which, as we have just emphasized, hides a further constraint on the shape of the state space.

3. Technological Aspects of DC-DC Converters

In DC-DC converter modeling and design, there exist several key concerns related to performance and reliability, including noise levels, switching losses, component stress, and output voltage ripple. Here is a general overview of each of these concerns:

1. Noise level:

DC-DC converters often involve rapid switching of currents and voltages, leading to electromagnetic interference. Electromagnetic interference can affect nearby electronic devices and may pose regulatory compliance challenges. Effective measures, such as shielding and filtering, are employed to mitigate EMI concerns [16]. In certain applications, the switching frequency or other factors can produce audible noise, which is undesirable. Design considerations include component and operational parameter selection to minimize audible noise.

2. Switching losses:

DC-DC converters experience losses during state transitions, such as switching between on/off states of thyristors. Such losses result in heat generation and reduced efficiency. Design optimization aims to minimize switching losses through careful component selection and control strategies [17,18].

3. Component stress:

Voltage and Current Stress: Components within DC-DC converters, such as diodes, capacitors, and inductors, endure high voltage and current stresses during operation. Component selection is crucial to ensure reliability by matching voltage and current ratings [19].

Thermal stress: Elevated temperatures may arise due to high switching frequencies and load conditions in DC-DC converters. Effective thermal management techniques, heat sinks, and component selection are employed to manage thermal stress and prevent component failure [20].

4. Output voltage ripple:

DC-DC converters are designed to provide a stable output voltage. However, due to switching and control dynamics, output voltage ripples may occur. Minimizing

output voltage ripple is crucial, especially in applications demanding precise voltage regulation [21]. There exist several strategies to mitigate output voltage ripple. The output voltage ripple is the ripple occurring across the capacitor C_2 and may be reduced, for a buck–boost converter, by an appropriate choice of the capacity C_2 , considering the switching rate and the rated output power. Output voltage ripple might be reduced through the application of output filters, such as inductors and capacitors, which serve to smooth the output voltage and enhance regulation. However, additional filters increase cost, size, and circuit complexity and are not a preferred choice in practice.

5. **Overshoot and undershoot:**

Overshoot refers to a temporary increase in the output voltage or current above the desired steady-state value when there is a sudden increase in load or input voltage. Rapid load increases lead the converter to momentarily produce a higher output voltage to meet the higher demand [22]. Sudden changes in input voltage, like voltage spikes or rapid increases, can also induce overshoot as the converter adjusts. Overshoot can potentially exceed component or load limits, causing damage or instability and may affect the performance of devices powered by the converter, particularly in sensitive applications.

Undershoot refers to a temporary decrease in the output voltage or current below the desired steady-state value when there is a sudden decrease in load or input voltage. A sudden reduction in load leads to undershoot as the converter momentarily produces a lower output voltage. Rapid changes in input voltage, especially when the control loop reacts slowly, can also result in undershoot [23]. Undershoot can lead to temporary power loss or a voltage drop, potentially disrupting connected devices or systems. In applications sensitive to voltage fluctuations, undershoot can cause data loss or system instability.

To manage overshoot and undershoot in DC-DC converters, practitioners employ various strategies. Proper design and tuning of the control loop are critical for responding optimally to load or input changes while minimizing transient deviations, selection of components with appropriate voltage and current ratings helps avoid component stress and enhance converter performance, implementation of input voltage surge protection mechanisms can reduce the impact of rapid input voltage changes, and voltage and current regulation feedback loops help to maintain stable output values and minimize overshoot and undershoot. In practice, the specific behavior of overshoot and undershoot depends on factors like the converter topology, control strategy, load conditions, and input voltage characteristics. Practitioners aim to strike a balance between achieving a fast response to load or input changes and minimizing these transient deviations to ensure reliable operation in their specific applications.

6. Stability issues:

Stability issues in DC-DC converters refer to concerns regarding the converter's ability to maintain a consistent and controlled output voltage or current under different operational conditions. These issues are essential for ensuring that the converter operates reliably without undesirable oscillations or instability [24].

Several factors influence stability in DC-DC converters. The choice of control strategy and the adjustment of control loop parameters significantly impacts stability, different DC-DC converter designs may exhibit varying levels of stability, rapid changes in the input voltage can challenge the converter's ability to maintain a stable output, sudden variations in the connected load can affect the converter's capacity to sustain a stable output, and component tolerances and properties, such as capacitance and inductance values, can also influence stability.

Proper design considerations, including selecting suitable components, minimizing parasitic elements, and optimizing the control loop, are critical for ensuring stability. Furthermore, experimental validation through real-world testing is essential to confirm stability under practical conditions, including varying loads and input voltages.

Engineers may employ control and compensation techniques, such as PID control or lead–lag compensation, to enhance stability.

Ultimately, the effective management of stability issues in DC-DC converters is crucial for guaranteeing their reliable and predictable performance across a range of applications.

In addressing such technological issues, engineers and researchers employ modeling and simulation techniques to analyze DC-DC converter performance. Factors such as switching topology selection, control strategy design, component choice, and layout optimization may be considered to enhance converter performance while satisfying specific application requirements. Furthermore, advancements in semiconductor technology and power electronics have led to the development of more efficient and reliable DC-DC converter designs in recent years.

As a theoretic control paper concerned with the development of a closed-loop control strategy, the present document does not consider such technical concerns any further.

4. Review of Control Design by Averaging on Lie Groups

The fundamental observation behind the solution proposed in [5] is related to the action of a Lie group on a smooth manifold. In the present case of interest, it boils down to the fact that every solution of the system (7) may be written as $x(t) = \Phi(t)x(0)$, where Φ represents a matrix-valued function that takes values in the special orthogonal group SO(3) of three-dimensional rotations and obeys the differential equation $\dot{\Phi} = (A + Bu)\Phi$ with initial condition $\Phi(0) = I$ and $t \in [0, t_f]$.

A first design choice is that the input signal u is taken as a concatenation of pulse trains. Each pulse switches between 0, in which it stays for $(1 - \mu)T$ secs, and 1, in which it stays for μT secs, where μ denotes the duty cycle and T the duration of each pulse (expressed in seconds). Each pulse train in the chain consists of a number of pulses, denoted as q. The design effort then consists in determining the total duration q of each train and the duty cycle μ for each train. Each pulse train consists possibly of a different number of pulses, which, upon adjusting their duration, may even be fractional.

Since a pulse train is a fast-oscillating periodic signal, it is assumed that the net effect of a pulse train is equivalent to that of its average. In other words, the effect of a fast-switching signal is assumed to be equivalent to that of its average $\overline{u} \in [0, 1]$. Under this assumption, it is possible to determine an approximate solution to the equation $\dot{\Phi} = (A + Bu)\Phi$.

The next design choice is to fix the final time t_f and to subdivide the interval $[0, t_f]$ into a number of sub-intervals, to which correspond some pre-specified points of the trajectory, which will then be followed by the system. By using the approximate solution to the equation $\dot{\Phi} = (A + Bu)\Phi$ within each sub-interval, it is therefore possible to make sure that the designed control *u* steers the system from the given initial state to the given final state along a pre-fixed trajectory.

Such a control design possesses a number of advantages, which may be summarized as follows:

- The conversion time t_f is pre-fixed and hence known in advance, which facilitates the integration of a converter into a more complex circuit.
- The trajectory over the state space may be optimized to fulfill further design constraints, such as keeping almost constant the current flowing through the inductor.
- Once the design of a converter is completed, its functioning is ensured by a solid theoretical background.

The method proposed in [5] clearly suffers from some drawbacks, which may be summarized as follows:

- The design is based on a number of arbitrary choices, such as the trajectory design.
- The actual computation of the pairs (μ, q) for each pulse train involves a non-linear optimization process that requires intensive computation (based on quaternions).

- The more accurate the averaging formulas required, the more complicated their implementation and usage.
- As an open-loop control algorithm was designed, it possesses no resiliency against parameter mismatch and modeling mismatch.

In the following, we shall propose a simpler, closed-loop control strategy that will be compared to the one devised by Leonard and Krishnaprasad.

5. Closed-Loop Control by a Criterion Function Optimization

Although buck, boost, buck–boost, and Ćuk converters were briefly revised, the present paper focuses on the buck–boost concept. As a matter of fact, Ćuk converters are of higher order compared to the other concepts [25], so a straightforward extension of the proposed method to control Ćuk converters would not be realistic.

In contrast to analog-type control based on high-frequency pulse-width modulation (PWM) actuation [12], in the present paper, digital control is envisaged. In fact, an assumption we make on the converter circuitry is that, once the switch has commuted from position 0 to 1 or from position 1 to 0, it cannot commute again before a given latency time, hereafter denoted as h > 0. Such an assumption implies that the signal u(t) is piecewise constant to either 0 or 1 able to change its value at most once every h seconds. Typically the value of h is far less than the unity (namely, $h \ll 1$).

An important consequence of the above assumption is that we may associate with the continuous-time signal u(t) a discrete-time sequence u_n defined as $u_n := u(nh)$, where n = 0, 1, 2, ..., N denotes a discrete-time index. In addition, since the input is piecewise constant, the state vector takes, within each interval [nh, (n + 1)h], a predictable value. In fact, within any such interval, the system (7) is of the type $\dot{x} = Fx$; hence, defining a discrete-time state vector sequence $x_n := x(nh)$, its solution reads $x_{n+1} = \exp(hF)x_n$ [26], where F is either A or A + B and 'exp' denotes matrix exponential. In other terms, it holds that

$$x_{n+1} = \begin{cases} \exp(hA)x_n & \text{if } u_n = 0, \\ \exp(h(A+B))x_n & \text{if } u_n = 1, \end{cases}$$
(10)

where $\exp(\cdot)$ denotes the matrix exponential. Since the state transition matrix is either $\exp(hA)$ or $\exp(h(A + B))$, it is appropriate to define

$$R^h_A := \exp(hA) \text{ and } R^h_{AB} := \exp(h(A+B)), \tag{11}$$

so that the state transition iteration (10) recasts as

$$x_{n+1} = \begin{cases} R_A^h x_n & \text{if } u_n = 0, \\ R_{AB}^h x_n & \text{if } u_n = 1. \end{cases}$$
(12)

Notice that both R_A^h , R_{AB}^h belong to the special orthogonal group SO(3) of threedimensional rotations, and hence the state transition $x_n \rightarrow x_{n+1}$ represents a threedimensional rotation that keeps unchanged the norm of each state vector instance. In fact, denoting by $R_n \in \{R_A^h, R_{AB}^h\}$ the *n*th transition matrix, the state transition from x_0 to x_N is due to a sequence of pure rotations, namely

$$x_N = R_N R_{N-1} R_{N-2} \dots R_2 R_1 R_0 x_0, \tag{13}$$

where $N := \lfloor t_f/h \rfloor$ denotes the duration of the conversion cycle in terms of the number of discrete steps.

In order to design a control sequence u_n that drives the state of the converter from x_0 to the desired state, which we shall denote as x_f , we shall make use of a method sometimes referred to as 'criterion function guidance', as explained, for example, in [27], based on the second method of Lyapunov. Such a control method is based on the definition of a criterion function *E* as a weighted distance between the current state and the desired state,

and in the development of an input control sequence that minimizes iteratively such a criterion function.

In the present work, we shall select as a criterion the function

$$E(x) := \frac{1}{2}(x - x_{\rm f})^{\top} P(x - x_{\rm f}), \tag{14}$$

where *P* denotes a symmetric, semi-positive definite 3×3 matrix. The quadratic criterion function *E* is defined as a squared weighted distance between the state and the desired state and has a measurement unit of V². The time-derivative $q_u(x) := \frac{dE}{dt}$ of such a criterion function reads

$$q_{u}(x) = (x - x_{f})^{\top} P \dot{x}$$

= $(x - x_{f})^{\top} P A x + u (x - x_{f})^{\top} P B x.$ (15)

The rate of decrease depends on the input u and the two possible decrease rates at state x read

$$\begin{cases} q_0(x) = (x - x_f)^{\top} PAx, \\ q_1(x) = (x - x_f)^{\top} P(A + B)x. \end{cases}$$
(16)

On the basis of such decrease rates, we may define the first instance of the control strategy as

(S1) if
$$\min\{q_0, q_1\} < 0$$
, then set $u = 0$ if $q_0 \le q_1$ or set $u = 1$ if $q_1 < q_0$.

Since it might happen that none of the control rates are negative, it is necessary to devise a second control strategy to apply in such event. We observe that during the first pulse, the switch must be in the position u = 0 to ensure that the inductor starts charging; during the conversion cycle, when there may be no energy transfer from the inductor to the storage capacitor, it is sensible to let the inductor charge by setting u = 0. Likewise, at the end of the conversion cycle, the switch must get back to the position u = 0 to ensure that the storage capacitor C_2 will not discharge into the inductor after having been charged to the fullest. On the basis of such reasoning, the second control strategy was devised as

(S2) if $\min\{q_0, q_1\} \ge 0$, then set u = 0.

The whole adopted control strategy is summarized in Figure 2.



Figure 2. Flowchart detailing the devised control strategy S1 + S2 to transfer the whole energy content of the source capacitor C_1 to the target energy storage C_2 .

We shall now assume the weighting matrix *P* to be diagonal, namely that

$$P = \begin{pmatrix} p_1 & 0 & 0\\ 0 & p_2 & 0\\ 0 & 0 & p_3 \end{pmatrix},$$
 (17)

with p_1 , p_2 , $p_3 \ge 0$. Under this assumption, we were able to estimate the time t^* at which the very first commutation takes place.

Theorem 2 (First commutation time). Define the unitless ratio $\rho := \frac{p_2\omega_2}{(p_1-p_3)\omega_1}$. Under the assumptions that $p_3 < p_1$, $h\omega_1 < \pi$, and $\rho < 1$, the exact time t^* at which the first commutation $0 \rightarrow 1$ of the control switch happens is given by

$$\omega_1 t^* = \cos^{-1}(\rho). \tag{18}$$

In addition, the state x^* reached at the first commutation reads $x^* = \sqrt{2E_0} (\rho \quad 0 \quad -\sqrt{1-\rho^2})^+$.

Proof. At the very beginning of the control cycle, it holds that

$$\begin{cases} q_0(x_0) = (x_0 - x_f)^\top P A x_0, \\ q_1(x_0) = (x_0 - x_f)^\top P (A + B) x_0. \end{cases}$$
(19)

Calculations reveal that

$$PAx_0 = (A+B)x_0 = 0, (20)$$

which implies that $q_0(x_0) = q_1(x_0) = 0$. Therefore, the first switch state is determined by strategy **S2**.

The first commutation $0 \rightarrow 1$ of the input control *u* will happen at a time $t^* > 0$. We further notice that after the first pulse, the control variables take the values

$$\begin{cases} q_0(x(h)) = (R_A^h x_0 - x_f)^\top PAR_A^h x_0 = -(p_1 - p_3)\omega_1 \cos(h\omega_1) \sin(h\omega_1)\sqrt{2E_0}, \\ q_1(x(h)) = (R_A^h x_0 - x_f)^\top P(A + B)R_A^h x_0 = -p_2\omega_2 \sin(h\omega_1)\sqrt{2E_0}. \end{cases}$$
(21)

Hence, as long as $p_3 < p_1$ and $h\omega_1 < \pi$, it holds that $q_0(x(h)) < 0$ and $q_1(x(h)) < 0$. Hence, within the first pulse, the criterion function decreases (i.e., the converter state gets closer to the desired state), and hence $t^* > h$.

The first commutation happens when the value of the function q_0 meets the value of the function q_1 ; hence, according to the devised strategy **S1**, the control input switches to 1. Such a condition corresponds to

$$0 = q_1 (e^{At^*} x_0) - q_0 (e^{At^*} x_0)$$

= $(e^{At^*} x_0 - x_f)^\top PBe^{At^*} x_0$
= $[(p_1 - p_3)\omega_1 \cos(\omega_1 t^*) - p_2 \omega_2)] \sin(\omega_1 t^*) \sqrt{2E_0}.$ (22)

The result (18) follows. The state x^* may be obtained by direct substitution of the value of t^* in the expression $\exp(At^*)x_0$. \Box

Notice that before the first commutation happens, the energy content of the capacitor C_2 is still null; hence, the first pulse train serves to load the magnetic field of the inductor. In addition, the commutation time t^* does not depend on the energy content E_0 .

It is instructive to observe that the ratio ρ depends on the non-zero entries of the weighting matrix P and on the ratio between the two capacitive elements, in fact $\omega_2/\omega_1 = \sqrt{C_1/C_2}$. In addition, it is worth observing that the weights p_1 and p_3 do not contribute independently of each other but only through their difference $p_1 - p_3$. For this reason, in the following, we shall always take $p_3 = 0$, which corresponds to leaving completely unconstrained the evolution of the current flowing through the inductor.

The advantages and drawbacks of the developed method in comparison to an openloop method, recalled in Section 4, are summarized in Table 1 for the convenience of the reader.

Table 1. Advantages and drawbacks of the proposed control strategy compared to the LK one.

Control Strategy	Advantages	Drawbacks
Leonard–Krishnaprasad Lie-group-averaging-based control strategy	Completes a conversion cycle in a pre-fixed time interval; specifies the trajectory in state space in advance (which may be optimized beforehand).	Assumes nominal values for the components; requires off-line computations to establish a control input sequence; requires re-calculation whenever changes in the conditions occur.
Proposed closed-loop feedback-type criterion-based control strategy	Deals with parameter mismatch as well as input/output voltage mismatch; requires no off-line computations to run; runs at lower switching frequency.	Does not guarantee a fixed conversion cycle duration; does not embody any limit on the intensity of the current flowing through the inductor.

6. Numerical Experiments and Comparison

In order to exemplify the behavior of the devised control algorithm and to compare its performances to those exhibited by the original LK algorithm, we shall present two series of experiments. The first series was performed under ideal conditions, while the second series was performed under pre-set value mismatch.

6.1. Comparisons under Nominal Conditions

In order to exemplify the performances of the devised control strategy, we shall repeat the numerical experiments conducted in [5] in order to be able to perform a comparison. The normalized values for the electrical components are $C_1 = 0.1$ Farad, $C_2 = 0.2$ Farad, $L_3 = 0.5$ Henry. In addition, we set $t_f = 1$ second and $E_0 = \frac{1}{2}$ joule. We shall mention, in our own interpretation of the choice of the authors of [5], that the considered circuit is 'normalized', namely the values of the capacitances and of the inductance are normalized by a factor several orders of magnitude less than the unit, since all that matters is ultimately the ratio C_1/C_2 .

In order to run the control algorithm, we set the pulse duration to h = 0.01 s and the weights to be $p_1 = 2$, $p_2 = 1$. With these values, we have $\rho \approx 0.3536$ and $t^* \approx 0.2704$ s.

The results obtained by the iteration (12) are displayed graphically in Figure 3.

The top panel of Figure 3 shows the sequence of pulse trains computed by the control algorithm of Figure 2. The control strategy resulting from the application of the devised algorithm is very clear. After a first long phase from t = 0 to $t = t^*$, in which the inductor loads its magnetic field of electrical energy, the inductor drains energy from the capacitor C_1 for short time intervals and subsequently cedes part of its energy to the capacitor C_2 , and this process repeats. The bottom panel of Figure 3 shows the evolution, over time, of the three state variables. In this panel, the vertical dashed line denotes the first commutation time t^* , while the horizontal dashed line denotes the value of the ratio ρ that the variable x_1 meets in correspondence of the first commutation time. The reached state at the end of the full conversion cycle was found to be $x_{100} = (0.0056 - 0.9998 \ 0.0176)^{\top}$, namely, the desired state x_f is reached with overall precision $\mathcal{O}(h)$. In fact, it is found that $\sqrt{(x_{100} - x_f)^{\top} P(x_{100} - x_f)} = \sqrt{2E(x_{100})} \approx 0.0068 \ J^{\frac{1}{2}}$, which denotes an overall measure of conversion precision. (Here, J stands for joule.)



Figure 3. Result of application of the devised control algorithm to the experimental setting of paper [5] with h = 0.01 s: pulse trains and state variable values.

Figure 4 illustrates the values taken by the criterion function and by the control variables during the control cycle.



Figure 4. Result of application of the devised control algorithm to the experimental setting of paper [5] with h = 0.01 s: control variables used by the devised algorithm.

The top panel shows the values of the criterion function *E* and of its derivative *E* during the control cycle. As expected, the criterion function *E* decreases monotonically to zero. The bottom panel shows the values of the control variables q_0 and q_1 , whose course meets the theoretical analysis.

In general, with the stated values for the electrical components of the converter, it is possible to predict the time t^* of the first $0 \rightarrow 1$ commutation as a function of the ratio p_2/p_1 . This dependence is shown in Figure 5, where the open circle corresponds to the ratio $p_2/p_1 = 1/2$ chosen for this experiment. The graphical result shows that it is possible to control the first commutation time fairly easily, if desired, by selecting the ratio p_2/p_1 .

By increasing the value of the latency time h, the precision of the conversion deteriorates, albeit not dramatically. Figure 6 illustrates the state trajectory of the converter when h = 0.02 s.



Figure 5. Dependence of the time t^* of the first $0 \rightarrow 1$ commutation as a function of the ratio p_2/p_1 .



Figure 6. Result of application of the devised control algorithm to the experimental setting of paper [5] with h = 0.02 s.

In this experiment, the reached state is $x_{50} = (0.0187 - 0.9986 \ 0.0503)^{\top}$, corresponding to an overall conversion precision of $\sqrt{2E(x_{50})} \approx 0.0201 \ \text{J}^{\frac{1}{2}}$.

Given the linearity of the system (7) in the state variables, the result of conversion is independent of the initial condition. By this we mean that an initial state $(\sqrt{2E_0} \ 0 \ 0)^{\top}$ will result in a final state close to $(0 - \sqrt{2E_0} \ 0)^{\top}$, for every $E_0 > 0$. The performance of the algorithm instead depends noticeably on the value of the constant *h*. For example, for a value $h = 10^{-4}$ s, the precision of conversion turns out to be approximately $5.2019 \times 10^{-5} \ J^{\frac{1}{2}}$.

Figure 7 illustrates the state trajectory and the switching sequence of the Leonard– Krishnaprasad method contrasted to the proposed control method. The state trajectories corresponding to the two methods differ substantially, especially the inductor current intensity. The overall evolution reveals comparable conversion performances obtained by a substantially different switching rate.



Figure 7. Comparison of the performances of the Leonard–Krishnaprasad (LK) and of the proposed methods on the experimental setting of paper [5] with h = 0.005 s.

As a further element of comparison, the number of $0 \rightarrow 1$ and $1 \rightarrow 0$ switchings were evaluated for both algorithms. These numbers, divided by the duration t_f of the conversion cycle, give the switching rate corresponding to the compared control algorithms. The LK method results in a switching rate of 117 Hz, in contrast to the proposed method, which entails a switching rate of 48 Hz. Such rates appear to be in good accordance with the results displayed in the bottom panels of Figure 7. We shall note that, as the values of the parameters are not realistic, the values of the switching rates are not realistic either; however, they serve for comparison purposes.

6.2. Comparison under Nominal Value Mismatch

In real-world settings, the values of the parameters of the electrical circuit in Figure 1 may not coincide with the nominal ones. In such an event, a closed-loop, feedback-driven algorithm is supposed to overperform a pre-set algorithm. The following numerical experiments aim to quantify the effects of parameter mismatch on the conversion performance and, ultimately, to assess the resilience of the considered control algorithms against parameter mismatch. The ideal values set in the tests were $C_1 = 0.1$ F, $C_2 = 0.2$ F, and $L_3 = 0.5$ H; therefore, $V_2(t_f) \approx \pm 0.7071V_1(0)$.

6.2.1. Mismatch in the Initial Source Voltage $V_1(0)$

The aim of the present set of experiments is to assess the entity of variation of the output voltage resulting from the variation of the source voltage. The results of three independent experiments are shown in Table 2. The percentage change in the output voltage as obtained by running both algorithms is less than 1% of its expected value, while being practically negligible for the proposed algorithm.

In addition, the adaptivity of the proposed algorithm allows us to attain conversion with fewer commutations of the switch (figures are omitted for brevity).

		Obtained Results			
Test Number	Initial Values	LK Algo	orithm	Proposed A	lgorithm
icst i uniber	initial values	Final Values	Deviation of Voltage V ₂	Final Values	Deviation of Voltage V ₂
First test	$V_1(0) = 2 V$ $V_2(0) = 0 V$ $I_3(0) = 0 A$	$V_1(1) = +0.0229 V$ $V_2(1) = -1.4055 V$ $I_3(1) = +0.1030 A$	-0.6%	$V_1(1) = -0.0001 \text{ V}$ $V_2(1) = -1.4142 \text{ V}$ $I_3(1) = +0.0062 \text{ A}$	~0.00%
Second test	$V_1(0) = 5 V$ $V_2(0) = 0 V$ $I_3(0) = 0 A$	$V_1(1) = +0.0573 \text{ V}$ $V_2(1) = -3.5138 \text{ V}$ $I_3(1) = +0.2575 \text{ A}$	-0.6%	$V_1(1) = -0.0003 V$ $V_2(1) = -3.5354 V$ $I_3(1) = +0.0155 A$	~0.00%
Third test	$V_1(0) = 7 V$ $V_2(0) = 0 V$ $I_3(0) = 0 A$	$V_1(1) = +0.0802 \text{ V}$ $V_2(1) = -4.9193 \text{ V}$ $I_3(1) = +0.3604 \text{ A}$	-0.6%	$V_1(1) = -0.0005 \text{ V}$ $V_2(1) = -4.9496 \text{ V}$ $I_3(1) = +0.0217 \text{ A}$	~0.00%

Table 2. Comparison of conversion results obtained by allowing a variation of the initial source voltage $V_1(0)$.

6.2.2. Mismatch in the Initial Output Voltage $V_2(0)$

In the present series of tests, the change in the V_2 output voltage, resulting from a non-zero initial voltage $V_2(0)$, is analyzed. Such tests aim at reproducing the presence of a residual voltage on the C_2 capacitor at the beginning of a conversion cycle. From the results of Table 3, it emerges that the percentage change of $V_2(1)$ pertaining to the proposed algorithm is lower.

Table 3. Comparison of conversion results obtained by allowing a variation of the initial output voltage $V_2(0)$.

		Obtained Results			
Test Number	Initial Values	LK Algorithm		Proposed Algorithm	
lest Number	initial values	Final Values	Deviation of Voltage V ₂	Final Values	Deviation of Voltage V ₂
First test	$V_1(0) = 1 V$ $V_2(0) = 0.5 V$ $I_3(0) = 0 A$	$V_1(1) = -0.4171 V$ $V_2(1) = -0.7521 V$ $I_3(1) = -0.1982 A$	6.36%	$V_1(1) = -0.4139 \text{ V}$ $V_2(1) = -0.7203 \text{ V}$ $I_3(1) = -0.2413 \text{ A}$	1.87%
Second test	$V_1(0) = 1 V$ $V_2(0) = 1 V$ $I_3(0) = 0 A$	$V_1(1) = -0.8457 V$ $V_2(1) = -0.8014 V$ $I_3(1) = -0.4480 A$	13.33%	$V_1(1) = -0.9751 V$ $V_2(1) = -0.7225 V$ $I_3(1) = -0.4484 A$	2.18%

6.2.3. Mismatch in the Initial Current $I_3(0)$

The aim of the present series of simulations is to quantify the variation of the final output voltage caused by variations of the initial inductor current $I_3(0)$. The purpose of these experiments is to analyze the performance of both algorithms in the event of a residual current in the L_3 inductor at the beginning of a conversion cycle.

From the results of Table 4, it emerges how the percentage variation of the output voltage $V_2(1)$ is lower when the proposed control algorithm is applied.

6.2.4. Large Mismatch in the Capacitance Values C₁ and C₂

The resilience of the analyzed control algorithms was assessed by recording the variation of the output voltage of the DC-DC converter resulting from large variations of the C_1 and C_2 values (far larger than commercial tolerance values). The purpose of this test is to analyze the performance of both algorithms in the event of a mistake in the choice of a single capacitor.

		Obtained Results			
Test Number	Initial Values	LK Algo	orithm	Proposed A	lgorithm
icst ivalliber	initial values	Final Values	Deviation of Voltage V ₂	Final Values	Deviation of Voltage V ₂
First test	$V_1(0) = 1 V$ $V_2(0) = 0 V$ $I_3(0) = 0.3 A$	$V_1(1) = -0.5453 V$ $V_2(1) = -0.7315 V$ $I_3(1) = -0.1982 A$	3.45%	$V_1(1) = -0.4881 \text{ V}$ $V_2(1) = -0.7209 \text{ V}$ $I_3(1) = -0.1856 \text{ A}$	1.95%
Second test	$V_1(0) = 1 V$ $V_2(0) = 0 V$ $I_3(0) = 0.5 A$	$ \begin{array}{l} V_1(1) = -0.9012 \ \mathrm{V} \\ V_2(1) = -0.7570 \ \mathrm{V} \\ I_3(1) = -0.2502 \ \mathrm{A} \end{array} $	7.06%	$V_1(1) = -0.9062 \text{ V}$ $V_2(1) = -0.7291 \text{ V}$ $I_3(1) = -0.4484 \text{ A}$	3.11%
Third test	$V_1(0) = 1 V$ $V_2(0) = 0 V$ $I_3(0) = -0.3 A$	$V_1(1) = -0.5224 V$ $V_2(1) = -0.6740 V$ $I_3(1) = +0.2325 A$	-4.68%	$V_1(1) = -0.5693 V$ $V_2(1) = -0.7208 V$ $I_3(1) = -0.1318 A$	1.94%

Table 4. Comparison of conversion results obtained by allowing a variation of the initial inductor current $I_3(0)$.

From the results displayed in Table 5, it appears that the effect of an incorrect choice in the capacitance value, when large, heavily affects the performance of the algorithms that control the DC-DC circuitry. Even in this case, however, the proposed algorithm shows a better resilience. In particular, the resilience against a large variation in the capacitance of the source capacitor C_1 is notable.

Table 5. Comparison of conversion results obtained by allowing a large variation of the capacitance of the capacitors C_1 and C_2 . In these simulation experiments, $V_1(0) = 1$ V, $V_2(0) = 0$ V, and $I_3(0) = 0$ A.

		Obtained Results			
Test Number	Components Values	LK Algo	LK Algorithm		lgorithm
lest Number	Components values	Final Values	Deviation of Voltage V ₂	Final Values	Deviation of Voltage V ₂
First test	$C_1 = 0.1 \text{ F}$ $C_2 = 0.4 \text{ F} (+100\%)$ $L_3 = 0.5 \text{ H}$	$V_1(1) = +0.0908 V$ $V_2(1) = -0.4659 V$ $I_3(1) = -0.1577 A$	-34.11%	$V_1(1) = +0.0453 \text{ V}$ $V_2(1) = -0.4957 \text{ V}$ $I_3(1) = -0.0551 \text{ A}$	-29.89%
Second test	$C_1 = 0.2 \text{ F} (+100\%)$ $C_2 = 0.2 \text{ F}$ $L_3 = 0.5 \text{ H}$	$V_1(1) = +0.4312 \text{ V}$ $V_2(1) = -0.9026 \text{ V}$ $I_3(1) = -0.0051 \text{ A}$	27.65%	$V_1(1) = -0.4989 V$ $V_2(1) = -0.7085 V$ $I_3(1) = -0.3156 A$	0.20%

6.2.5. Large Mismatch in the Values of the Inductance L_3

The aim of these further simulations is to assess the variation of the output voltage at the end of a conversion cycle resulting from a mismatch in the value of the inductance.

From the results of Table 6, it is clear that the percentage variation of the voltage $V_2(1)$ is lower with the proposed algorithm in all considered cases. The proposed closed-loop algorithm proved henceforth to be more resilient than the pre-fixed LK algorithm.

6.2.6. Five Percent Tolerance in the Values of the Parameters of the Discrete Components

A five percent tolerance in the values of the parameters C_1 , C_2 , and L_3 may be expected in yield components, which would result in a degradation of conversion performances.

From the results of Table 7, it emerges that in response to a small mismatch of single components, the proposed algorithm works better in terms overall results compared to the LK one.

		Obtained Results				
Test Number	Components Values	LK Algo	orithm	Proposed A	lgorithm	
lest ivumber	Components values	Final Values	Deviation of Voltage V ₂	Final Values	Deviation of Voltage V ₂	
First test	$C_1 = 0.1 \text{ F}$ $C_2 = 0.2 \text{ F}$ $L_3 = 0.1 \text{ H} (-80\%)$	$V_1(1) = +0.6298 V$ $V_2(1) = +0.5262 V$ $I_3(1) = +0.2339 A$	-174.41%	$V_1(1) = +0.0106 \text{ V}$ $V_2(1) = -0.7070 \text{ V}$ $I_3(1) = -0.0149 \text{ A}$	-0.01%	
Second test	$C_1 = 0.1 \text{ F}$ $C_2 = 0.2 \text{ F}$ $L_3 = 0.8 \text{ H} (+60\%)$	$V_1(1) = -0.2614 \text{ V}$ $V_2(1) = -0.6506 \text{ V}$ $I_3(1) = -0.1036 \text{ A}$	-7.99%	$V_1(1) = -0.0003 V$ $V_2(1) = -0.6891 V$ $I_3(1) = -0.0792 A$	-2.55%	
Third test	$C_1 = 0.1 \text{ F}$ $C_2 = 0.2 \text{ F}$ $L_3 = 1 \text{ H} (+100\%)$	$V_1(1) = +0.3737 \text{ V}$ $V_2(1) = -0.5874 \text{ V}$ $I_3(1) = -0.1307 \text{ A}$	-16.93%	$V_1(1) = -0.0179 \text{ V}$ $V_2(1) = -0.6343 \text{ V}$ $I_3(1) = -0.1397 \text{ A}$	-10.30%	

Table 6. Comparison of conversion results obtained by allowing a large variation of the inductance L_3 of the inductor. In these simulation experiments, $V_1(0) = 1$ V, $V_2(0) = 0$ V, and $I_3(0) = 0$ A.

Table 7. Comparison of conversion result degradation due to a mismatch in the values of the discrete components of $\pm 5\%$. In these simulation experiments, $V_1(0) = 1$ V, $V_2(0) = 0$ V, and $I_3(0) = 0$ A.

		Obtained Results			
Test Number	Components Values	LK Algo	orithm	Proposed A	lgorithm
	Components values	Final Values	Deviation of Voltage V ₂	Final Values	Deviation of Voltage V ₂
First test	$C_1 = 0.105 \text{ F} (+5\%)$ $C_2 = 0.2 \text{ F}$ $L_3 = 0.5 \text{ H}$	$V_1(1) = +0.0457 \text{ V}$ $V_2(1) = -0.7205 \text{ V}$ $I_3(1) = +0.0466 \text{ A}$	1.90%	$V_1(1) = -0.1643 \text{ V}$ $V_2(1) = -0.7078 \text{ V}$ $I_3(1) = -0.0628 \text{ A}$	0.10%
Second test	$C_1 = 0.095 \text{ F} (-5\%)$ $C_2 = 0.2 \text{ F}$ $L_3 = 0.5 \text{ H}$	$V_1(1) = -0.0251 \text{ V}$ $V_2(1) = -0.6835 \text{ V}$ $I_3(1) = +0.0567 \text{ A}$	-3.34%	$V_1(1) = +0.0034 \text{ V}$ $V_2(1) = -0.6892 \text{ V}$ $I_3(1) = -0.0018 \text{ A}$	-2.53%
Third test	$C_1 = 0.1 \text{ F}$ $C_2 = 0.210 \text{ F} (+5\%)$ $L_3 = 0.5 \text{ H}$	$V_1(1) = +0.0020 V$ $V_2(1) = -0.6884 V$ $I_3(1) = +0.0343 A$	-2.65%	$V_1(1) = -0.0163 \text{ V}$ $V_2(1) = -0.6898 \text{ V}$ $I_3(1) = +0.0108 \text{ A}$	-2.45%
Fourth test	$C_1 = 0.1 \text{ F}$ $C_2 = 0.190 \text{ F} (-5\%)$ $L_3 = 0.5 \text{ H}$	$V_1(1) = +0.0218 \text{ V}$ $V_2(1) = -0.7168 \text{ V}$ $I_3(1) = +0.0699 \text{ A}$	1.37%	$V_1(1) = -0.1753 \text{ V}$ $V_2(1) = -0.7091 \text{ V}$ $I_3(1) = +0.0525 \text{ A}$	0.28%
Fifth test	$C_1 = 0.1 \text{ F}$ $C_2 = 0.2 \text{ F}$ $L_3 = 0.525 \text{ H} (+5\%)$	$V_1(1) = +0.0366 \text{ V}$ $V_2(1) = -0.7056 \text{ V}$ $I_3(1) = +0.0277 \text{ A}$	-0.21%	$V_1(1) = +0.0088 \text{ V}$ $V_2(1) = -0.7068 \text{ V}$ $I_3(1) = +0.0123 \text{ A}$	-0.04%
Sixth test	$C_1 = 0.1 \text{ F}$ $C_2 = 0.2 \text{ F}$ $L_3 = 0.475 \text{ H} (-5\%)$	$V_1(1) = -0.0143 \text{ V}$ $V_2(1) = -0.6970 \text{ V}$ $I_3(1) = +0.0786 \text{ A}$	-1.42%	$V_1(1) = +0.0057 \text{ V}$ $V_2(1) = -0.7070 \text{ V}$ $I_3(1) = +0.0063 \text{ A}$	-0.01%

6.2.7. Ten Percent Tolerance in the Values of the Parameters of the Discrete Components

Further to the previous section, a larger tolerance of ten percent in the values of the parameters of the discrete components, in line with commercial standards, may be taken as a basis for comparison of conversion performances.

The obtained results are displayed in Table 8, from which it emerges how in response to a higher mismatch of single components, the percentage variation of the final output voltage $V_2(1)$ stays proportional to the results obtained in Table 7. Again, it is clear how the proposed algorithm provides better results compared to the LK algorithm.

		Obtained Results				
Test Number	Components Values	LK Algo	orithm	Proposed A	lgorithm	
	Components values	Final Values	Deviation of Voltage V ₂	Final Values	Deviation of Voltage V ₂	
First test	$C_1 = 0.11 \text{ F} (+10\%)$ $C_2 = 0.2 \text{ F}$ $L_3 = 0.5 \text{ H}$	$V_1(1) = +0.0778 V$ $V_2(1) = -0.7368 V$ $I_3(1) = +0.0421 A$	4.20%	$V_1(1) = -0.2178 \text{ V}$ $V_2(1) = -0.7130 \text{ V}$ $I_3(1) = -0.0789 \text{ A}$	0.83%	
Second test	$C_1 = 0.09 \text{ F} (-10\%)$ $C_2 = 0.2 \text{ F}$ $L_3 = 0.5 \text{ H}$	$V_1(1) = -0.0640 \text{ V}$ $V_2(1) = -0.6625 \text{ V}$ $I_3(1) = +0.0624 \text{ A}$	-6.31%	$V_1(1) = +0.0093 V$ $V_2(1) = -0.6708 V$ $I_3(1) = -0.0006 A$	-5.13%	
Third test	$C_1 = 0.1 \text{ F}$ $C_2 = 0.22 \text{ F} (+10\%)$ $L_3 = 0.5 \text{ H}$	$V_1(1) = +0.0066 \text{ V}$ $V_2(1) = -0.6740 \text{ V}$ $I_3(1) = -0.0182 \text{ A}$	-4.68%	$V_1(1) = +0.0163 \text{ V}$ $V_2(1) = -0.6740 \text{ V}$ $I_3(1) = +0.0074 \text{ A}$	-4.68%	
Fourth test	$C_1 = 0.1 \text{ F}$ $C_2 = 0.18 \text{ F} (-10\%)$ $L_3 = 0.5 \text{ H}$	$V_1(1) = +0.0333 \text{ V}$ $V_2(1) = -0.7303 \text{ V}$ $I_3(1) = +0.0895 \text{ A}$	3.28%	$V_1(1) = -0.2792 \text{ V}$ $V_2(1) = -0.7102 \text{ V}$ $I_3(1) = -0.0533 \text{ A}$	0.44%	
Fifth test	$C_1 = 0.1 \text{ F}$ $C_2 = 0.2 \text{ F}$ $L_3 = 0.55 \text{ H} (+10\%)$	$V_1(1) = +0.0610 \text{ V}$ $V_2(1) = -0.7061 \text{ V}$ $I_3(1) = -0.0068 \text{ A}$	-0.14%	$V_1(1) = +0.0079 \text{ V}$ $V_2(1) = -0.7069 \text{ V}$ $I_3(1) = +0.0089 \text{ A}$	-0.03%	
Sixth test	$C_1 = 0.1 \text{ F}$ $C_2 = 0.2 \text{ F}$ $L_3 = 0.45 \text{ H} (-10\%)$	$V_1(1) = +0.0404 \text{ V}$ $V_2(1) = -0.6876 \text{ V}$ $I_3(1) = -0.1096 \text{ A}$	-2.76%	$V_1(1) = +0.0141 \text{ V}$ $V_2(1) = -0.7069 \text{ V}$ $I_3(1) = +0.0098 \text{ A}$	-0.03%	

Table 8. Comparison of conversion result degradation due to a mismatch in the values of the discrete components of $\pm 10\%$. In these simulation experiments, $V_1(0) = 1$ V, $V_2(0) = 0$ V, and $I_3(0) = 0$ A.

6.2.8. Combined Ten Percent Variation of the Values of the Parameters C₁ and C₂

In contrast to the case when just one of the components is subject to a mismatch in its nominal value, conversion performances are evaluated when the values of both capacitors are subjected to mismatch at the same time.

The results obtained by running both algorithms are displayed in Table 9, from which it is clear how the proposed algorithm yields better results than the LK one. When, in particular, the capacitance mismatch exhibits opposite signs (+10%/-10% or -10%/+10%), both algorithms decrease in performance. This is due to the fact that the final output value is strictly correlated to the capacitor ratio, based on Formula (5).

Table 9. Combined ten percent variation of the values of the parameters C_1 and C_2 . In these simulation experiments, $V_1(0) = 1$ V, $V_2(0) = 0$ V, and $I_3(0) = 0$ A.

		Obtained Results				
Test Number	Components Values	LK Algo	orithm	Proposed A	lgorithm	
lest Number	components values	Final Values	Deviation of Voltage V ₂	Final Values	Deviation of Voltage V ₂	
First test	$C_1 = 0.11 \text{ F} (+10\%)$ $C_2 = 0.2 \text{ F}$ $L_3 = 0.5 \text{ H}$	$V_1(1) = +0.0778 V$ $V_2(1) = -0.7368 V$ $I_3(1) = +0.0421 A$	4.20%	$V_1(1) = -0.2178 \text{ V}$ $V_2(1) = -0.7130 \text{ V}$ $I_3(1) = -0.0789 \text{ A}$	0.83%	
First test	$\begin{array}{l} C_1 = 0.11 \ \mathrm{F} \ (+10\%) \\ C_2 = 0.22 \ \mathrm{F} \ (+10\%) \\ L_3 = 0.5 \ \mathrm{H} \end{array}$	$V_1(1) = +0.0610 \text{ V}$ $V_2(1) = -0.7061 \text{ V}$ $I_3(1) = +0.0075 \text{ A}$	-0.14%	$V_1(1) = +0.0079 \text{ V}$ $V_2(1) = -0.7069 \text{ V}$ $I_3(1) = -0.0098 \text{ A}$	-0.03%	
Second test	$\begin{array}{l} C_1 = 0.11 \ \mathrm{F} \ (+10\%) \\ C_2 = 0.18 \ \mathrm{F} \ (-10\%) \\ L_3 = 0.5 \ \mathrm{H} \end{array}$	$V_1(1) = +0.0981 \text{ V}$ $V_2(1) = -0.7664 \text{ V}$ $I_3(1) = -0.0817 \text{ A}$	8.39%	$V_1(1) = -0.3667 \text{ V}$ $V_2(1) = -0.7175 \text{ V}$ $I_3(1) = -0.0714 \text{ A}$	1.47%	

		Obtained Results			
Test Number	Components Values	LK Algo	rithm	Proposed A	lgorithm
lest ivumber	components values	Final Values	Deviation of Voltage V ₂	Final Values	Deviation of Voltage V ₂
Third test	$C_1 = 0.09 \text{ F} (-10\%)$ $C_2 = 0.22 \text{ F} (+10\%)$ $L_3 = 0.5 \text{ H}$	$V_1(1) = -0.0836 V$ $V_2(1) = -0.6361 V$ $I_3(1) = +0.0307 A$	-10.04%	$V_1(1) = +0.0232 \text{ V}$ $V_2(1) = -0.6394 \text{ V}$ $I_3(1) = -0.0044 \text{ A}$	-9.57%
Fourth test	$C_1 = 0.09 \text{ F} (-10\%)$ $C_2 = 0.18 \text{ F} (-10\%)$ $L_3 = 0.5 \text{ H}$	$V_1(1) = -0.0404 \text{ V}$ $V_2(1) = -0.6876 \text{ V}$ $I_3(1) = +0.0986 \text{ A}$	-2.76%	$V_1(1) = +0.0141 \text{ V}$ $V_2(1) = -0.7069 \text{ V}$ $I_3(1) = +0.0088 \text{ A}$	-0.03%

Table 9. Cont.

6.2.9. Combined Ten Percent Component Variation

The last series of simulated tests aim at assessing the resilience of the control algorithms when all discrete components are subjected to a ten percent change with respect to their nominal values. The obtained results are displayed Table 10.

Table 10. Combined ten percent variation of the values of all components. In these simulation experiments, $V_1(0) = 1$ V, $V_2(0) = 0$ V, and $I_3(0) = 0$ A.

		Obtained Results				
Test Number	Components Values	LK Algo	orithm	Proposed A	lgorithm	
	components values	Final Values	Deviation of Voltage V ₂	Final Values	Deviation of Voltage V ₂	
First test	$\begin{array}{l} C_1 = 0.11 \ \mathrm{F} \ (+10\%) \\ C_2 = 0.18 \ \mathrm{F} \ (-10\%) \\ L_3 = 0.55 \ \mathrm{H} \ (+10\%) \end{array}$	$V_1(1) = +0.1435 \text{ V}$ $V_2(1) = -0.7718 \text{ V}$ $I_3(1) = +0.0337 \text{ A}$	9.15%	$V_1(1) = -0.3522 \text{ V}$ $V_2(1) = -0.7103 \text{ V}$ $I_3(1) = -0.1003 \text{ A}$	0.45%	
Second test	$\begin{array}{l} C_1 = 0.11 \ \mathrm{F} \ (+10\%) \\ C_2 = 0.18 \ \mathrm{F} \ (-10\%) \\ L_3 = 0.45 \ \mathrm{H} \ (-10\%) \end{array}$	$V_1(1) = +0.0503 \text{ V}$ $V_2(1) = -0.7475 \text{ V}$ $I_3(1) = +0.1436 \text{ A}$	5.71%	$V_1(1) = +0.3987 \text{ V}$ $V_2(1) = -0.7152 \text{ V}$ $I_3(1) = -0.0308 \text{ A}$	1.15%	
Third test	$\begin{array}{l} C_1 = 0.09 \ \mathrm{F} \ (-10\%) \\ C_2 = 0.18 \ \mathrm{F} \ (-10\%) \\ L_3 = 0.55 \ \mathrm{H} \ (+10\%) \end{array}$	$V_1(1) = +0.0064 \text{ V}$ $V_2(1) = -0.7019 \text{ V}$ $I_3(1) = +0.0510 \text{ A}$	-0.74%	$V_1(1) = +0.0069 \text{ V}$ $V_2(1) = -0.7070 \text{ V}$ $I_3(1) = +0.0047 \text{ A}$	-0.01%	
Fourth test	$\begin{array}{l} C_1 = 0.09 \ \mathrm{F} \ (-10\%) \\ C_2 = 0.18 \ \mathrm{F} \ (-10\%) \\ L_3 = 0.45 \ \mathrm{H} \ (-10\%) \end{array}$	$V_1(1) = -0.0877 \text{ V}$ $V_2(1) = -0.6585 \text{ V}$ $I_3(1) = +0.1591 \text{ A}$	-6.87%	$V_1(1) = +0.0031 \text{ V}$ $V_2(1) = -0.7071 \text{ V}$ $I_3(1) = -0.0031 \text{ A}$	~0.00%	
Fifth test	$\begin{array}{l} C_1 = 0.09 \; \mathrm{F} \; (-10\%) \\ C_2 = 0.22 \; \mathrm{F} \; (+10\%) \\ L_3 = 0.55 \; \mathrm{H} \; (+10\%) \end{array}$	$V_1(1) = -0.0306 V$ $V_2(1) = -0.6394 V$ $I_3(1) = -0.0114 A$	-9.57%	$V_1(1) = +0.0122 \text{ V}$ $V_2(1) = -0.6396 \text{ V}$ $I_3(1) = +0.0000 \text{ A}$	-9.55%	
Sixth test	$\begin{array}{l} C_1 = 0.09 \ \mathrm{F} \ (-10\%) \\ C_2 = 0.22 \ \mathrm{F} \ (+10\%) \\ L_3 = 0.45 \ \mathrm{H} \ (-10\%) \end{array}$	$V_1(1) = -0.1386 \text{ V}$ $V_2(1) = -0.6219 \text{ V}$ $I_3(1) = +0.0857 \text{ A}$	-12.04%	$V_1(1) = +0.0207 \text{ V}$ $V_2(1) = -0.6395 \text{ V}$ $I_3(1) = +0.0018 \text{ A}$	-9.56%	

From the obtained results it appears that the proposed algorithm shows better performance than the LK algorithm.

7. Conclusions and Devised Extensions

The purpose of the illustrated research was to propose a novel control strategy for a prototypical DC-DC electrical converter on the basis of an early work by Leonard and Krishnaprasad, where a DC-DC converter was modeled as a state space dynamical system and controlled by an open-loop strategy based on Lie group theory. In the present research endeavor, we have introduced a closed-loop control strategy based on two criteria, namely maximum convergence rate and minimal energy exchange. A theoretical study of the time where the first commutation $0 \rightarrow 1$ of the switch happens was conducted. A series of numerical simulations were shown and examined to illustrate the devised control algorithm. The novel method was compared to the original one by Leonard and Krishnaprasad numerically.

We shall underline that the intention of the paper was mostly a theoretical speculation, without a direct connection to normal DC-DC converter operation, along the same lines as the reference paper [5]. In fact, an operation mode of a DC-DC converter does not imply that an input capacitor C_1 is discharged into an output capacitor C_2 . In contrast, the design and operation (and control) of a converter is based on a practically constant voltage V_1 , while the voltage V_2 exhibits a voltage ripple influenced by control and by the value of the capacitor C_2 . Additionally, in the considered case study, no load is connected to the output of the converter, whereas in practical applications, an electrical load is certainly present.

A possible extension of the devised method would be that of a single source to multiple target storage unit (SS2MTU), namely to transfer the energy content of a source capacitor C_s to a number of target capacitors C_i , with i = 1, 2, ..., N with different capacitive elements so as to achieve different conversion ratios simultaneously.

A further extension, building on the SS2MSU system, would be a multiple DC source to a multiple DC storage unit (MSU2MTU), possibly with different capacitance values, to accommodate for a variety of concurring DC energy sources being converted to a multiple storage unit with possibly different conversion ratios.

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References

- 1. Li, Z.; Soh, Y.; Wen, C. (Eds.) Switched and Impulsive Systems: Analysis, Design and Applications; Springer: Berlin/Heidelberg, Germany, 2005.
- 2. Sun, Z.; Ge, S.S. (Eds.) Switched Linear Systems: Control and Design; Springer: Berlin/Heidelberg, Germany, 2005.
- 3. Liberzon, D. Switching in Systems and Control; Birkhäuser: Basel, Switzerland, 2006.
- 4. Mahmoud, M.S. Switched Time-Delay Systems: Stability and Control; Springer: Berlin/Heidelberg, Germany, 2010.
- Leonard, N.; Krishnaprasad, P. Control of switched electrical networks using averaging on Lie groups. In Proceedings of 1994 33rd IEEE Conference on Decision and Control, Orlando, FL, USA, 14–16 December 1994; Volume 2, pp. 1919–1924. [CrossRef]
- Corradini, L.; Maksimovic, D.; Mattavelli, P.; Zane, R. Digital Control of High-Frequency Switched-Mode Power Converters; John Wiley & Sons: Hoboken, NJ, USA, 2015.
- Kursun, V.; Narendra, S.; De, V.; Friedman, E. Low-voltage-swing monolithic DC-DC conversion. IEEE Trans. Circuits Syst. II Express Briefs 2004, 51, 241–248. [CrossRef]
- 8. Mohan, N.; Undeland, T.M.; Robbins, W.P. *Power Electronics: Converters, Applications, and Design,* 3rd ed.; John Wiley & Sons: Hoboken, NJ, USA, 2005.
- 9. Shen, C.L.; Shen, Y.S.; Tsai, C.T. Isolated DC-DC converter for bidirectional power flow controlling with soft-switching feature and high step-up/down voltage conversion. *Energies* **2017**, *10*, 296. [CrossRef]
- Drakunov, S.V.; Reyhanoglu, M.; Singh, B. Sliding mode control of DC-DC power converters. *IFAC Proc. Vol.* 2009, 42, 237–242. [CrossRef]
- Sira-Ramirez, H.; Rios-Bolivar, M. Sliding mode control of DC-to-DC power converters via extended linearization. *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.* **1994**, 41, 652–661. [CrossRef]
- 12. Tan, S.C.; Lai, Y.; Cheung, M.; Tse, C. On the practical design of a sliding mode voltage controlled buck converter. *IEEE Trans. Power Electron.* **2005**, *20*, 425–437. [CrossRef]

- 13. Hingorani, N. Flexible AC transmission. IEEE Spectr. 1993, 30, 40-45. [CrossRef]
- Rudervall, R.; Charpentier, J.P.; Sharma, R.Y. High voltage direct current (HVDC) transmission systems technology review paper. In Proceedings of the Energy Week, Washington, DC, USA, 7–8 March 2000.
- 15. Fiori, S.; Di Filippo, R. An improved chaotic optimization algorithm applied to a DC electrical motor modeling. *Entropy* **2017**, *19*, 665. [CrossRef]
- 16. Subramanian, A.; Govindarajan, U. Analysis and mitigation of conducted EMI in current mode controlled DC–DC converters. *IET Power Electron.* **2019**, 12, 667–675. [CrossRef]
- Mondzik, A.; Piróg, S.; Stala, R.; Penczek, A.; Gucwa, P. DC-DC boost converter with reduced switching losses in wide range of voltage gain. *Energies* 2023, 16, 4397. [CrossRef]
- Zhang, K.; Shan, Z.; Jatskevich, J. Estimating switching loss and core loss in dual active bridge DC-DC converters. In Proceedings of the 2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL), Vancouver, BC, Canada, 12–15 July 2015; pp. 1–6. [CrossRef]
- 19. Gitau, M.N.; Masike, L.; Adams, G.P. A unified analysis of DC-DC converters's current stress. Energies 2023, 16, 3370. [CrossRef]
- 20. Kishor, Y.; Patel, R. Thermal modelling and reliability analysis of recently introduced high gain converters for PV application. *Clean. Energy Syst.* **2022**, *3*, 100016. [CrossRef]
- Kuisma, M.; Jarvelainen, T.; Silventoinen, P. Analyzing voltage ripple in variable-frequency DC/DC boost converter. In Proceedings of the 2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551), Aachen, Germany, 20–25 June 2004; Volume 2, pp. 1085–1089. [CrossRef]
- Li, H.; Liu, Q.; Zhang, Z.; Jiang, X.; Cao, G.; Zhang, Y. A voltage vershoot design method for DC-DC converter based on state overshoot concept. In Proceedings of the IECON 2021—47th Annual Conference of the IEEE Industrial Electronics Society, Toronto, ON, Canada, 13–16 October 2021; pp. 1–6. [CrossRef]
- Cao, J.; Chen, B.; Ye, H.; Feng, J. A peak-current mode boost converter with fast linear transient response. *Microelectron. J.* 2023, 139, 105897. [CrossRef]
- Hamidi, S.A.; Nasiri, A. Stability analysis of a DC-DC converter for battery energy storage system feeding CPL. In Proceedings of the 2015 IEEE International Telecommunications Energy Conference (INTELEC), Osaka, Japan, 18–22 October 2015; pp. 1–5. [CrossRef]
- 25. Gholizadeh, H.; Gorji, S.A.; Afjei, E.; Sera, D. Design and implementation of a new Cuk-based step-up DC–DC converter. *Energies* **2021**, *14*, 6975. [CrossRef]
- Moler, C.; Van Loan, C. Nineteen dubious ways to compute the exponential of a matrix, twenty-five years later. SIAM Rev. 2003, 45, 3–49. [CrossRef]
- 27. Lopez, I.; McInnes, C.R. Autonomous rendezvous using artificial potential function guidance. J. Guid. Control. Dyn. 1995, 18, 237–241. [CrossRef]

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