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A Compact and Robust Technique for the Modeling and Parameter Extraction of Carbon Nanotube Field Effect Transistors

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Received: 26 October 2020; Accepted: 16 December 2020; Published: 20 December 2020

Abstract: Carbon nanotubes field-effect transistors (CNTFETs) have been recently studied with great interest due to the intriguing properties of the material that, in turn, lead to remarkable properties of the charge transport of the device channel. Downstream of the full-wave simulations, the construction of equivalent device models becomes the basic step for the advanced design of high-performance CNTFET-based nanoelectronics circuits and systems. In this contribution, we introduce a strategy for deriving a compact model for a CNTFET that is based on the full-wave simulation of the 3D geometry by using the finite element method, followed by the derivation of a compact circuit model and extraction of equivalent parameters. We show examples of CNTFET simulations and extract from them the fitting parameters of the model. The aim is to achieve a fully functional description in Verilog-A language and create a model library for the SPICE-like simulator environment, in order to be used by IC designers.

Keywords: carbon nanotubes; field-effect transistors; finite element method; parameter extraction; device modeling; circuit; SPICE

1. Introduction

An intrinsic carbon nanotube (CNT) under a low voltage bias is characterized by ballistic or near-ballistic transport related to the very long mean free path. This quasi one-dimensional (1D) structure provides improved electrostatic control over the channel region with respect to the 3D (e.g., bulk CMOS) and 2D devices. The above properties place the carbon-nanotube field-effect transistors (CNTFETs) among the best candidate devices for extending or complementing traditional silicon CMOS IC technology. Thus, recently, the research and interest of CNTFETs have been continuously growing owing to their high potential for future applications.

The 1D transport and the consequent low scattering rate of charge carriers in CNTs could easily grant low noise, low power dissipation, and low signal distortion due to the inherently high linearity of the current–voltage characteristics [1]. In addition, chemical stability and high thermal dissipation could further promote CNT as one of the possible building blocks for carbon based electronics [2–4].

A computationally efficient and accurate compact model describing the CNTFET behavior is of paramount importance in the design of analog circuit applications for communication systems.

Thus far, most CNTFET compact models have been developed for digital circuit design. For analog circuit design, an efficient and compact model needs to satisfy several stringent requirements such as high-order continuity of all bias-dependent model equations and smooth geometry scaling. Additionally, the extraction of (geometrical and non geometrical) parameters is typically more demanding and complex.

Deng et al. [5] presented for the intrinsic channel region of a MOSFET-like single-walled CNTFET a compact and efficient circuit model. The proposed CNTFET model is valid for large variations in CNT chirality and diameter and for CNTFET with either metallic or semiconducting CNT active region (channel). It represents an excellent starting point toward a general CNTFET model that implements at a circuit level a number or practical device non-idealities (such as the elastic scattering in the channel region, the resistive doped source/drain, the Schottky-barrier resistance, and the parasitic gate capacitances) with HSPICE [6].

In [7], a compact and efficient CNTFET model focusing on both intrinsic and extrinsic device properties (e.g., tunneling current and parasitic capacitances) was firstly introduced for future implementation in SPICE or Verilog-A. It is based on the virtual-source (VS) approach consisting of a semi-empirical model applicable to MOSFETs and depending on a large amount of reproducible data to extract device empirical parameters [8]. In the latter work, the CNTFET empirical parameters were related to the device geometries and structures, such as gate and contact length, to enable projections that reflect changes in the device design, while the remaining parameters were extracted from a few sets of experimental data. This model captures CNTFET physical properties which are relevant in the circuit design and optimization.

In [9], the intrinsic elements of a compact CNTFET model based on the VS modeling were developed. The model is able to consider the dimensional scaling effects and can be used to evaluate the influence of the CNT diameter on the intrinsic device performance. The VS-CNTFET model was implemented in Verilog-A, and it can run smoothly in SPICE or SPICE-like environments because all the equations are analytical with no numerical iterations, and the output current is differentiable throughout all the operating regions.

Finally, a more comprehensive analysis that includes the non-ideal contacts and tunneling leakage effects was implemented in [10]

In the present work, we propose a compact and versatile model for the analysis and simulation of the FET, based on the following steps: (i) full-wave modeling of a given architecture (3D geometry and related technology files) by using a finite element solver based on the combination of COMSOL Multiphysics and MATLAB. The active region, e.g., the channel is an assembly of semiconductive nanotubes, be they single-wall (SW) or multi-wall (MW). In this region, (ii) we solve the Schrödinger equation and derive the charge transport for the CNT layer(s) of given size, chirality, intrinsic doping, and kind of contacts with metal electrodes. We can deal with the ballistic regime, as well as extend the model to the limit of a diffusive (non ballistic) regime [11]. The output results of the 3D full-wave simulations are the input data for deriving the customized equivalent circuit model. In particular, (iii) we modify the virtual-source CNTFET (VS-CNTFET) model in [9,10] in order to fit it to the COMSOL implementation of the proposed CNTFET architecture. Self-consistently, (iv) we extract from the simulation results the physical (geometrical) and non-physical (fitting) parameters for the customized virtual source CNTFET SW model in order to obtain a Verilog-A description of this model suitable for analog circuit design.

2. Full-Wave Simulation

We consider a typical configuration of a CNTFET, whose geometry and material parameters (see Table 1) are of the order of magnitude of the fabricated devices reported in [12–14]. We built up a computational platform in which we interface (i) the full-wave COMSOL solver together with (ii) a Poisson–Schrödinger home-made solver. The former (i) deals with complex geometries together

with material properties, the latter (ii) allows for solving self-consistently the Poisson–Schrödinger equation (written in MATLAB) in the CNT active region.

Table 1. VS-CNTFET model input parameters.

Name	Description	Type
s	spacing between the CNTs (center-to-center) (m)	geometrical
W	transistor width (m)	geometrical
L_g	physical gate length (m)	geometrical
H_g	gate height (m)	geometrical
L_c	contact length (m)	geometrical
L_{ext}	source/drain extension length or spacer length (m)	geometrical
d	CNT diameter (m)	geometrical
t_{ox}	gate oxide thickness (m)	physical
k_{ox}	gate oxide dielectric constant	physical
k_{cnt}	CNT dielectric constant	physical
k_{sub}	substrate dielectric constant	physical
k_{spa}	source/drain spacer dielectric constant	physical
E_{fsd}	Fermi level to the band edge (eV) at the source/drain, related to the doping density	physical
V_{fb}	flat band voltage (V) (for threshold voltage adjustment)	physical
Geo_{mod}	device geometry	geometrical
Rc_{mod}	contact mode	physical
R_{s0}	user-defined series resistance (Ω)	physical
SDT_{mod}	source-to-drain tunneling (SDT) mode	physical
$BTBT_{mod}$	band-to-band tunneling mode	physical
T	temperature (°C)	physical

The Poisson's equation along the tube is solved by COMSOL and is written as follows:

$$\frac{d^2V}{d\rho^2} + \frac{1}{\rho}\frac{dV}{d\rho} + \frac{dV}{dy^2} = \frac{Q}{\epsilon} \tag{1}$$

where V is the electric potential, $\rho = \sqrt{x^2 + z^2}$ is the radial distance from the symmetry axis of the tube, y is the direction parallel to the symmetry axis, Q is the nanotube linear charge density, and ϵ is the dielectric constant of the tube.

While the steady-state Schrödinger equation is given by:

$$\frac{d^2\psi_{h,e}}{dy^2} = -\frac{2m}{\hbar^2}(E - U_{h,e})\psi_{h,e} \tag{2}$$

in which $\psi_{h,e}$ is the wave-function of holes/electrons, m is the effective mass of the particle, $\hbar$ is the reduced Planck constant, and E represents the energy of the particle displaced inside an electric potential $U_{h,e}$. The above mathematical platform is able to provide a self-consistent description of electron/holes transport [1] by means of a transmission line formalism modeling the carrier–waves propagation and their coupling to the external end self-induced voltage.

The model geometry consists of a 10 nm thick single slice W of the whole device, with periodic conditions along the x-axis direction. A defined potential is applied to the metal contacts; in the tube region, the space charge density is defined, while, for the remaining domains, a charge conservation condition is imposed. Figure 1 shows the analysed CNTFET geometrical configuration.

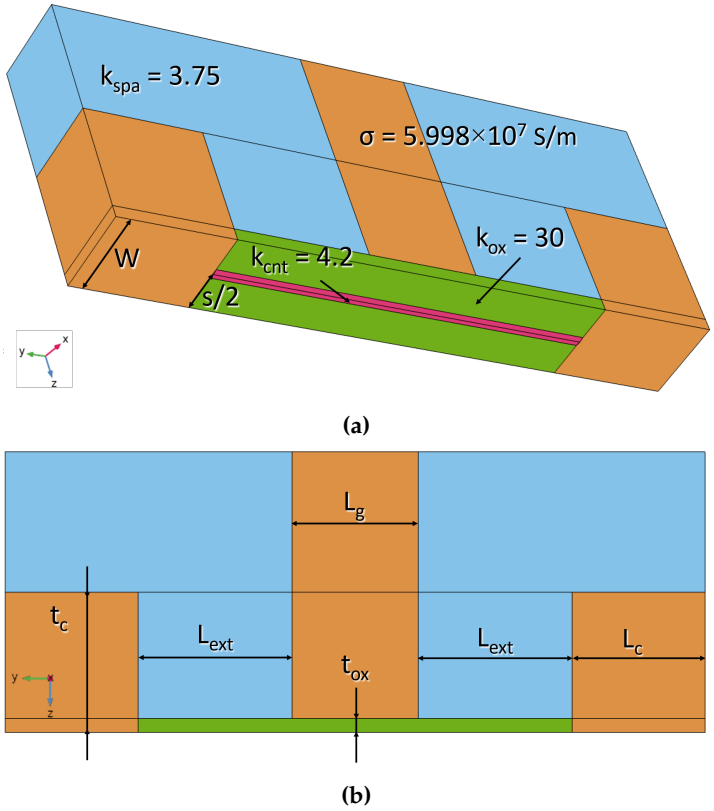

Figure 1. The analysed geometrical configuration of a CNTFET in (**a**) 3D view and (**b**) 2D view. Details: gate, source and drain contacts (orange), filler material (cyan), gate oxide (green) and the nanotube (magenta). The parameters are described in Table 1.

Data computation proceeds as follows:

1. The MATLAB procedure calculates the charge inside the tube, considering a null electric potential, and then provides it to COMSOL as an input;
2. COMSOL calculates the electric potential in each point of the device, including the nanotube;
3. The electric potential along the tube is provided to the MATLAB procedure, then the loop is repeated until convergence is reached.

Regarding the choice of the full-wave COMSOL solver as a simulation method for the CNTFET process, we specify that the full-3D simulation used as a numerical reference is characterized by some specific approximations or ideal assumptions in relation to charge transport in the CNT channels, such as, for instance, less crystal defects and the absence of substrate effects. However, the COMSOL platform, for self-consistent calculation of charge transport in carbon nanotubes, is a powerful tool that can account, in principle, for several parasitic effects, such as stray capacitances, current leakage, and cross-coupling between different CNTs. Additionally, the CNTFET can be characterized both in DC conditions and at high operation frequency, for large bandwidth characterization. However, COMSOL is not the only tool used to perform our calculations, in fact, in order to provide a more accurate and complete modeling of the device, the above simulations include, in the same computational framework, many quantum effects, such as carrier interference, tunneling, self-consistent potential, coupling with metal contacts, and contribution of quantum capacitance/resistance, owing to a direct live-link to Fortran and MATLAB in-house code, which is particularly suited for coherent transport analysis, as widely reported in previous work (e.g., [1]). Such kind of analysis in mainly needed to provide a starting point for calibration and numerical tests of compact models of CNTFETs, but further extension will be possible in the near future, with the additional contribution of experimental data.

3. Formulation of the Compact CNTFET Model

Various carbon nanotube FET (CNTFET) models have been reported in recent years [15–22]; however, some of them use simplifications, making it questionable when evaluating the transient response and device dynamic performance, while other models are described in terms of an integral function that requires intensive calculation efforts, making it difficult to implement in circuit simulators like SPICE. Recently, two very effective models for CNT have been developed at Stanford [5,6,9,10]: (i) a circuit-compatible SPICE model for CNTFET, (ii) a compact virtual source model for CNTFET. A brief description of these two models is reported in the following.

3.1. A Circuit Compatible SPICE Model for CNTFET

In this case, the device modeling has been developed with reference to the 3D structure of CNTFET illustrated in Figure 2.

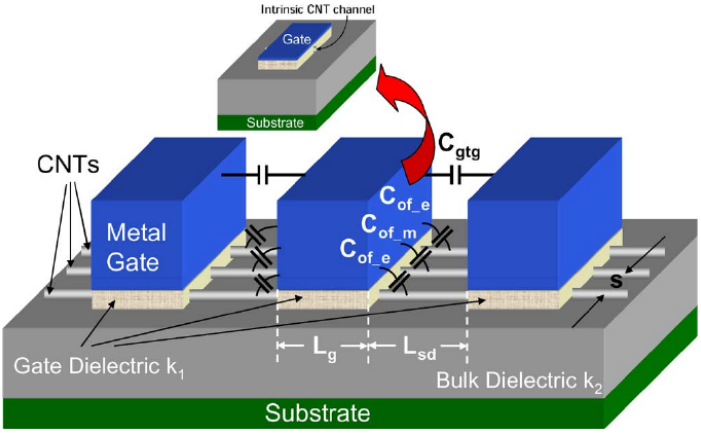

Figure 2. 3D structure of CNTFET. © [2007] IEEE. Reprinted, with permission, from [5].

The model is described hierarchically in three levels, as shown in Figure 3.

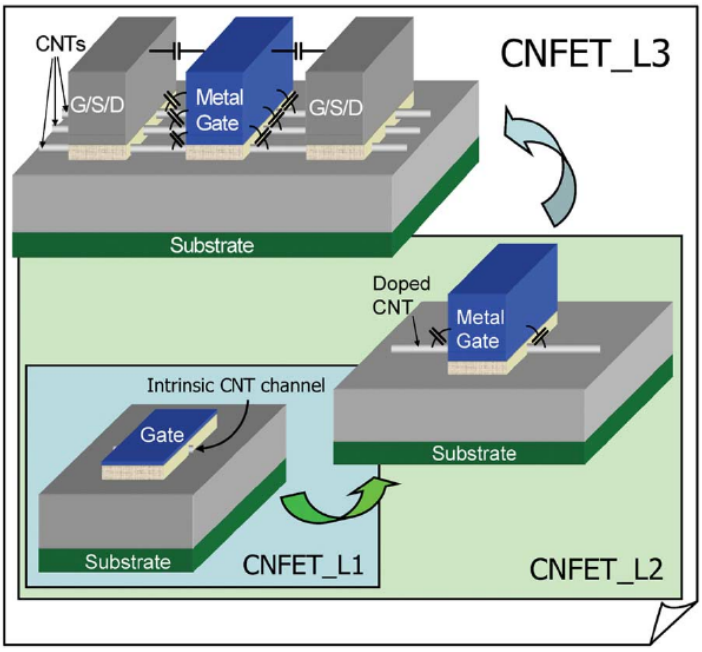

Figure 3. The model is described hierarchically in three levels. © [2007] IEEE. Reprinted, with permission, from [6].

Level 1 models the intrinsic behavior of CNTFET. Level 2 includes the device level non idealities, i.e.,: defect/impurity scattering in the channel region; quantum wires resistance; parasitic capacitance of the doped source/drain region; Schottky barrier (SB) resistance between the doped CNT and the S/D metal contacts. Level 3 refers to multiple CNTs, and includes the parasitic gate capacitance and screening effect due to adjacent CNTs. Here, a synthetic review of the first level alone will be reported.

CNTFET Device Model Level 1

Level 1, denoted as CNTFET_L1, models the intrinsic behavior of CNTFET with a near-ballistic transport and without any parasitic capacitance and parasitic resistance. The equivalent circuit model is shown in Figure 4 and includes three current sources: (1) the thermionic current contributed by the semiconducting subbands (I_{semi}) with the classical band theory; (2) the current contributed by the metallic subbands (I_{metal}); and (3) the leakage current (I_{btbt}) caused by the band-to-band tunneling (BTBT) mechanism through the semiconducting subbands.

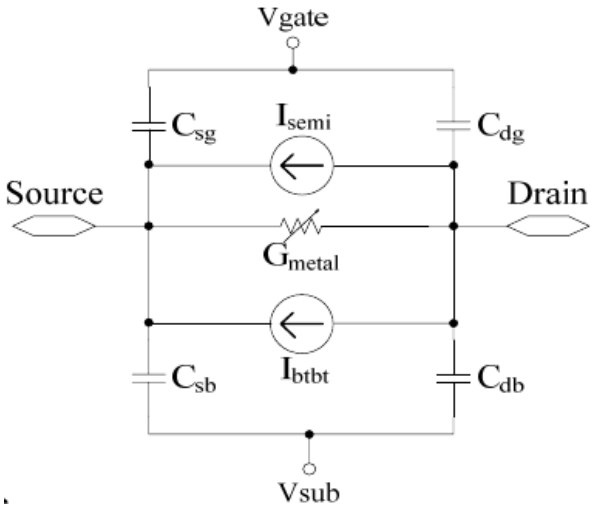

Figure 4. The 1st level equivalent circuit model CNTFET_L1 for CNTFET. © [2007] IEEE. Reprinted, with permission, from [5].

Here, we summarize the modeling for the I_{semi} component.

I_{semi}: For semiconducting subbands, the current contributed by the substate (m, l) is given by

$$J_{m,l}(V_{xs}, \Delta\Phi_B) = \frac{2e}{h} \frac{\sqrt{3}a\pi V_\pi}{L_g} \frac{k_l}{\sqrt{k_m^2 + k_l^2}} \frac{1}{1 + e^{(E_{m,l} + eV_{xs} - \Delta\Phi_B)/kT}} \tag{3}$$

where V_{xs} is the potential difference between the node x and source, $\Delta\Phi_B$ is the channel surface-potential lowering with gate/drain bias, L_g the channel length, V_π (~ 3.033 eV) the carbon $\pi - \pi$ bond energy in the tight binding model, k_m the wave number of the m th subband, k_l the wave number of the l th substate, $E_{(m,l)}$ the carrier energy at the substate (m, l). The total current contributed by all substates is equal to the current flowing from the drain to the source (corresponding to $+k$ branch, i.e., positive velocity) minus the current flowing from the source to the drain (corresponding to $-k$ branch):

$$I_{semi}(V_{ch,DS}, V_{ch,GS}) = 2 \sum_{\substack{k_m \\ m=1}}^{M} \sum_{\substack{k_l \\ l=1}}^{L} [T_{LR} J_{m,l}(0, \Delta\Phi_B)|_{+k} - T_{RL} J_{m,l}(V_{ch,DS}, \Delta\Phi_B)|_{-k}] \tag{4}$$

where $V_{ch,DS}$ and $V_{ch,GS}$ represent the Fermi potential differences near the drain and within the channel, T_{LR} and T_{RL} are the transmission probability of the carrier at the substate (m, l) in $+k$ and

$-k$ branches, respectively. The channel surface-potential charge $\Delta\Phi_B$ can be calculated using the charge conservation equation

$$Q_{cap}(\Delta\Phi_B) = Q_{CNT}(\Delta\Phi_B) \tag{5}$$

where Q_{cap} is the charge induced by the electrodes, and Q_{CNT} is the total charge induced on the CNT surface. Due to the nonlinearity of Q_{CNT}, (5) is solved iteratively by the equation solver reported in Figure 5.

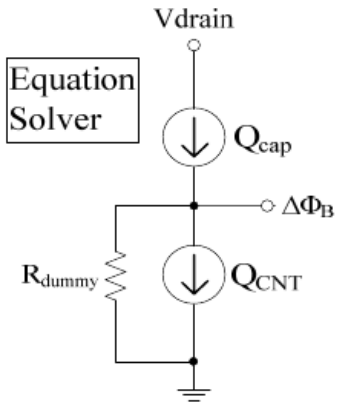

Figure 5. Equation solver implemented in SPICE. © [2007] IEEE. Reprinted, with permission, from [5].

3.2. A Compact Virtual-Source Model for CNT

The virtual-source (VS) model is a semi-empirical model that contains only a few physical parameters, and assumes the current depends on a gate-controlled source-injection barrier [9,10]. The model was initially developed for short-channel Si MOSFET [8,23] and subsequently adapted for CNTFETs. Based on the VS approach, the drain current (I_D) of a MOSFET is the product of the mobile charge density and the carrier velocity at the VS, i.e., at the location of the top of the energy barrier ($x = x_0$) between the source and the channel (see Figure 6).

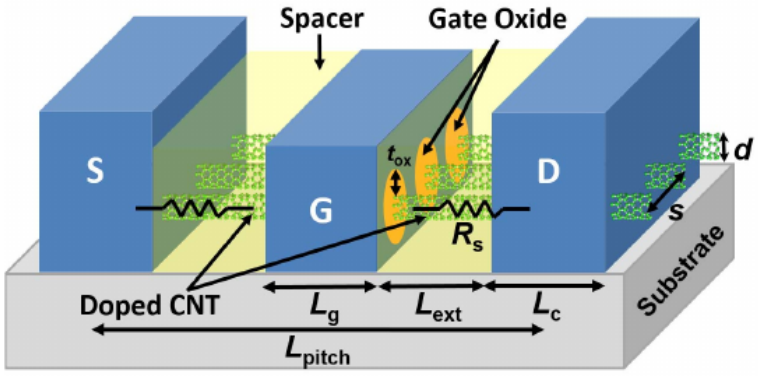

Figure 6. A representative 3D gate-all-around CNTFET structure used in the VS-CNTFET model. © [2015] IEEE. Reprinted, with permission, from [9].

The model is specified by ten parameters: (1) gate length (L_g); (2) gate capacitance in strong inversion region (C_{inv}); (3) low-field effective mobility (μ); (4) threshold voltage (V_t); (5) inverse subthreshold slope factor (n); (6) drain-induced barrier lowering (DIBL) coefficient (δ); (7) series resistance (R_S); (8) VS carrier velocity (v_{xo}); (9) fitting parameter α; and (10) fitting parameter β used to smooth the transitions between weak and strong inversion, and between non-saturation and saturation regions, respectively.

The model was derived by distinguishing two regions of operation: *(a)* saturation, *(b)* non-saturation.

a. VS model in saturation

In this case, the drain current normalized by width (I_D/W) of a MOSFET can be described by

$$I_D/W = Q_{ixo}\, v_{xo} \tag{6}$$

where

$$Q_{ixo} = C_{inv}\, n\, \phi_t \ln\left(1 + \exp\frac{V'_{GS} - (V_t - \alpha\, \phi_t\, F_f)}{n\, \phi_t}\right) \tag{7}$$

and the function F_f is a Fermi function that allows for a smooth transition between the two values of reference voltage. C_{inv} is the effective gate-to-channel capacitance per unit area in strong inversion, ϕ_t is the thermal voltage ($k_B T/q$), V'_{GS} is the internal gate-source voltage, i.e., corrected for the voltage drop on the source R_S and is given by $V'_{GS} = V_{GS} - I_D R_s$, n is the subthreshold coefficient, which is related to the so-called subthreshold swing (SS) by $SS = n\, \phi_T$. The threshold voltage V_t is given by

$$V_t = V_{to} - \delta V'_{DS} \tag{8}$$

where δ is the drain-inducted-barrier-lowering (DIBL) coefficient that introduces dependency of Q_{ixo} on V_{DS}, V_{to} is the strong-inversion threshold voltage at $V_{DS} = 0$, V'_{DS} accounts for the voltage drop on both R_S and R_D (drain resistance) as $V'_{DS} = V_{DS} - I_D(R_S + R_D)$.

b. VS model in non-saturation

In this region, the current is expressed by

$$I_D/W = Q_{ixo} v_{xo} F_S \tag{9}$$

where F_S is a saturation function defined by

$$F_S = \frac{V'_{DS}/V_{DSAT}}{(1 + (V'_{DS}/V_{DSAT})^{\beta})^{1/\beta}} \tag{10}$$

which increases smoothly from 0, at $V'_{DS} = 0$, to 1, at $V'_{DS} > V_{DSAT}$, where V_{DSAT} is the saturation voltage

$$V_{DSAT} = \frac{v_{xo} L_c}{\mu} \tag{11}$$

and $L_c = L_g - 2L_{ov}$ is the effective channel length obtained from the gate length, accounting for source and drain overlap (L_{ov}).

VS Model for CNTFET

On the basis of VS approach [8], a model for CNTFET has been developed [9] by deriving expressions for the VS parameters as functions of device dimensions and CNT diameter (d), which is a crucial parameter because it determines the CNT band structure and the bandgap (E_G). As an example in the VS-CNTFET model, C_{inv} is calculated as follows:

$$\begin{aligned} C_{inv} &= C_{ox} C_{qeff}/(C_{ox} + C_{qeff}) \\ C_{qeff} &= c_{qa}\sqrt{qE_g/(k_B T)} + c_{qb} \\ C_{ox} &= 2\pi k_{ox}\varepsilon_0/\{\ln[(2t_{ox} + d)/d]\} \end{aligned} \tag{12}$$

where q is the elementary charge, c_{qa} and c_{qb} are the empirical fitting parameters, C_{ox} is the gate oxide capacitance, ε_0 is the permittivity in vacuum, and t_{ox} and k_{ox} are the thickness and the relative dielectric constant at the gate oxide, respectively.

The VS carrier velocity (v_{xo}) can be associated with L_g through the theory of back scattering of carriers in the channel, thus giving

$$v_{xo} = \frac{\lambda_v}{\lambda_v + 2l} v_B \tag{13}$$

where v_B is the carrier velocity in the ballistic limit, λ_v is the carrier MFP, and l is the critical length defined as the distance over which the electric potential drops by $k_B T/q$ from the top of the energy barrier in the channel.

4. Results and Discussion

4.1. Model Fitting

The proposed method aims to modify a "base" model in order to fit it to the COMSOL implementation of the proposed CNTFET architecture and to obtain a Verilog-A description of the final customized virtual source CNTFET SW model suitable for analog circuit design. This can be done through the extraction and modeling of the physical (geometrical) and non-physical (fitting) parameters of the "base" model starting from experimental data derived from COMSOL simulation of the CNTFET architecture described in Section 2. The idea is to extract and modify these parameters using a fitting algorithm that minimizes the difference between the predicted data and the real data obtained from COMSOL simulation. When the minimum error has been reached, the obtained values can be used in the next step: the optimization of the SPICE device, initially built on the "base" model values, and now described with the fitted values, in order to fit the given architecture and thus realize the customized virtual source CNTFET SW model.

The first step has been to find this "base" model that is to find an equivalent model of the CNTFET, to get a model description in Verilog-A language [24] in order to create a model library and consequently a component in the Cadence environment. This equivalent model is the VS-CNTFET model described in Section 3.2. This model has both a Verilog-A description, suitable for circuit design, and an equivalent MATLAB description, useful for experimentation, both available online [25].

About the experimental data, these data have been obtained from COMSOL simulations of the CNTFET architecture described in Section 2.

Regarding the model fitting algorithm, an experimentation of accurate model fitting techniques exploring different approaches has been carried, but the simulated annealing algorithm [26,27] has shown the best performance for our application.

Simulated annealing (SA) is a probabilistic technique for solving optimization problems, which aims to find a global minimum when there are multiple local minima. The SA algorithm models the physical process of heating a material followed by cooling through a slow lowering of the temperature that decreases defects, thus, minimizing the system energy, SA randomly generates a new point at each iteration. The distance of the new point from the current point is based on a probability distribution proportional to the temperature. As the algorithm proceeds, an annealing schedule is selected to systematically decrease the temperature and, as the temperature decreases, the algorithm reduces the extent of its search to converge to a minimum.

The chosen objective function is the minimization of the root mean square of the difference between the estimated current and the real current given from COMSOL data.

A description of the implemented framework is shown in Figure 7.

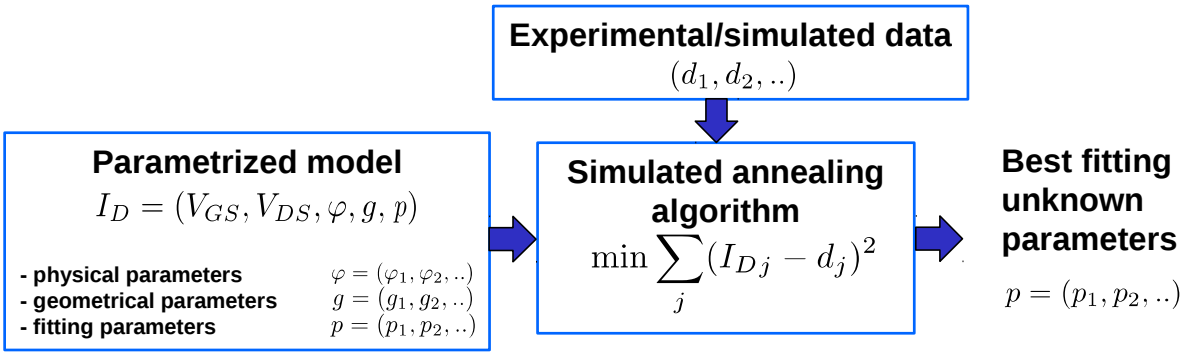

Figure 7. Model fitting flowchart.

Inputs to the VS-CNTFET are design-related parameters such as the gate length (L_g), contact length (L_c), CNT diameters (d), and gate oxide thickness (t_{ox}), as listed in Table 1. Some of these parameters are well-defined from the COMSOL CNTFET architecture as reported in Table 2 and can be directly modified in the VS-CNTFET model, but most of the parameters in Table 1 are specific for the VS-CNTFET default implementation and need to be modified in order to fit the COMSOL implementation of the proposed CNTFET architecture.

In Table 2, we specify W = 1 µm instead of W = 10 nm as in Figure 1 because we assume, for the fitting simulations, a number of CNTs in the device $Ncnt = W/s = 100$, with s = 10 nm, supposing no-border effect.

Table 2. Input parameters of the 3D full-wave simulation model.

Name	Value
s	10 nm
W	1 µm
L_g	90 nm, 190 nm, 290 nm
L_{ext}	5 nm
d	1.26 nm
t_{ox}	10 nm
k_{ox}	30
k_{cnt}	4.2
k_{spa}	3.75
E_{fsd}	0.5557 eV
Geo_{mod}	top-gate
SDT_{mod}	off
$BTBT_{mod}$	on
T	16.85 °C (290 K)

As mentioned in Section 3.2, the VS-CNTFET model is characterized by the parameters summarized in Table 3. Regarding the geometrical parameter L_g that is the gate length, we choose a priori three values for our architecture, as reported in Table 2, so this parameter is fixed and does not belong to the fitting variables. However, in addition to the VS-CNTFET fitting parameters, we also fit the parameters c_{qa} and c_{qb}, in order to obtain the quantum capacitance C_{qeff}. Particularly, we need to extract from the model these parameters that, in the Verilog-A (or MATLAB) implementation, are embedded in the model. All these values can be used to optimize the SPICE representation of the device.

Table 3. Fitting parameters for the customized virtual source CNTFET SW model.

Name	Description
C_{inv}	gate capacitance in strong inversion region (F/m)
μ	low-field effective mobility ($m^2V^{-1}s^{-1}$)
V_t	threshold voltage (V)
n (SS)	inverse subthreshold slope factor (V/dec)
δ (DIBL)	drain-induced barrier lowering coefficient (V/V)
R_S	series resistance (Ω)
v_{xo}	VS carrier velocity (m/s)
c_{qa}	CNT quantum capacitance param 1 (F/m)
c_{qb}	CNT quantum capacitance param 2 (F/m)

4.2. Simulations Results

Starting from a MATLAB implementation of the VS-CNTFET model and the experimental data obtained from COMSOL simulations of the given CNTFET architecture, an experimentation has been carried out in order to reach the minimum error, first fitting a few parameters and gradually increasing the parameters of the VS-CNTFET model. The developed framework, based on the SA algorithm, automatically performs the fitting of multi-parameters of the model.

Once the minimum error has been reached, the obtained values can be used in the final step: the optimization of the SPICE device, initially based on VS-CNTFET model values, and now described with the fitted values, in order to fit the given CNTFET architecture. Thus, a Verilog-A model description suitable for analog circuit design has been obtained.

Figures 8–10 report the current/voltage characteristic (I_D-V_{DS}) as a function of V_{GS} for different values of L_g and V_{GS} values from 0.4 V to 0.75 V with a step size of 0.05 V, showing the effectiveness of the proposed approach. As you can see, the I_D-V_{DS} curves obtained with the model fitting framework reaches a low error compared with the curves derived from COMSOL data.

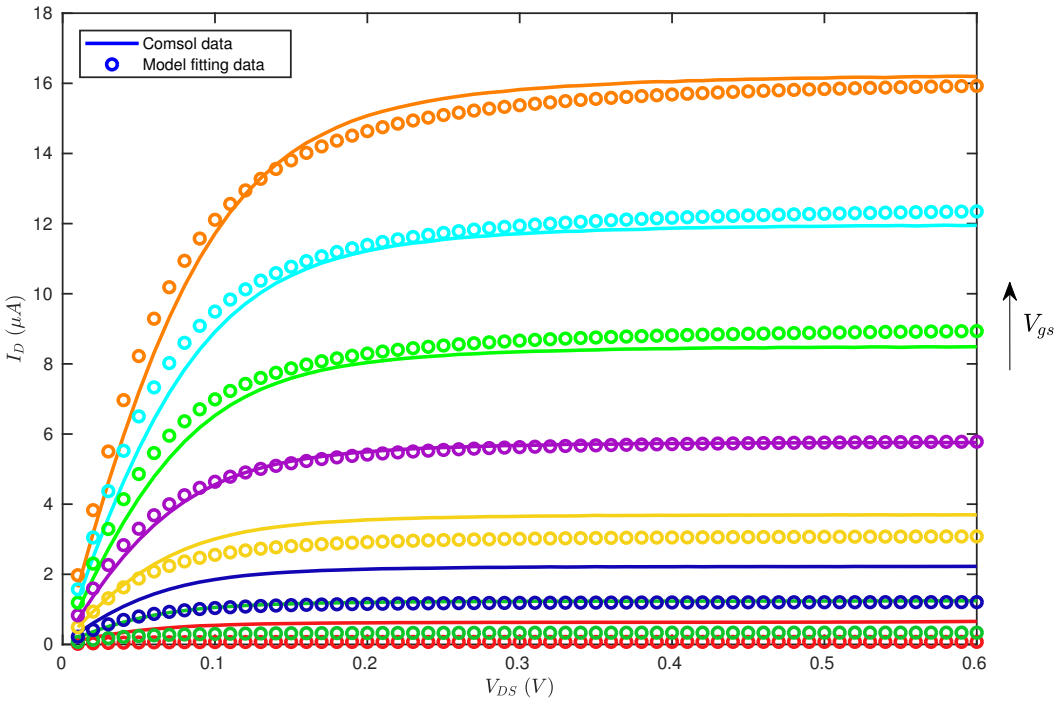

Figure 8. Best model fitting with $L_g = 90$ nm and V_{GS} values from 0.4 V to 0.75 V, with a step size of 0.05 V.

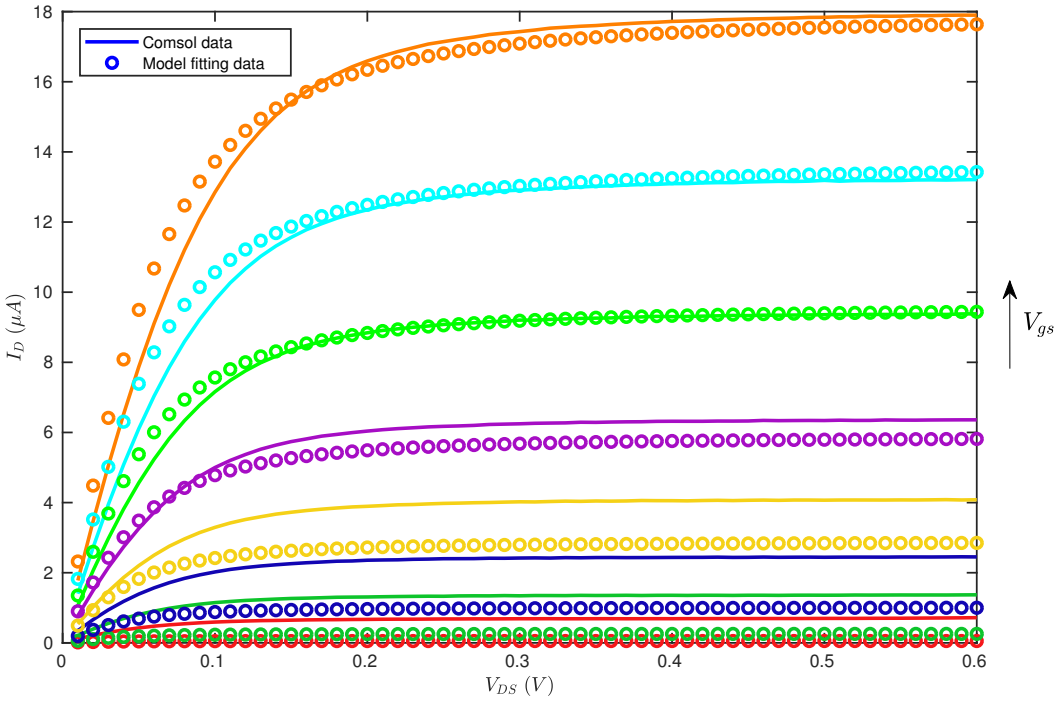

Figure 9. Best model fitting with $L_g = 190$ nm and V_{GS} values from 0.4 V to 0.75 V, with a step size of 0.05 V.

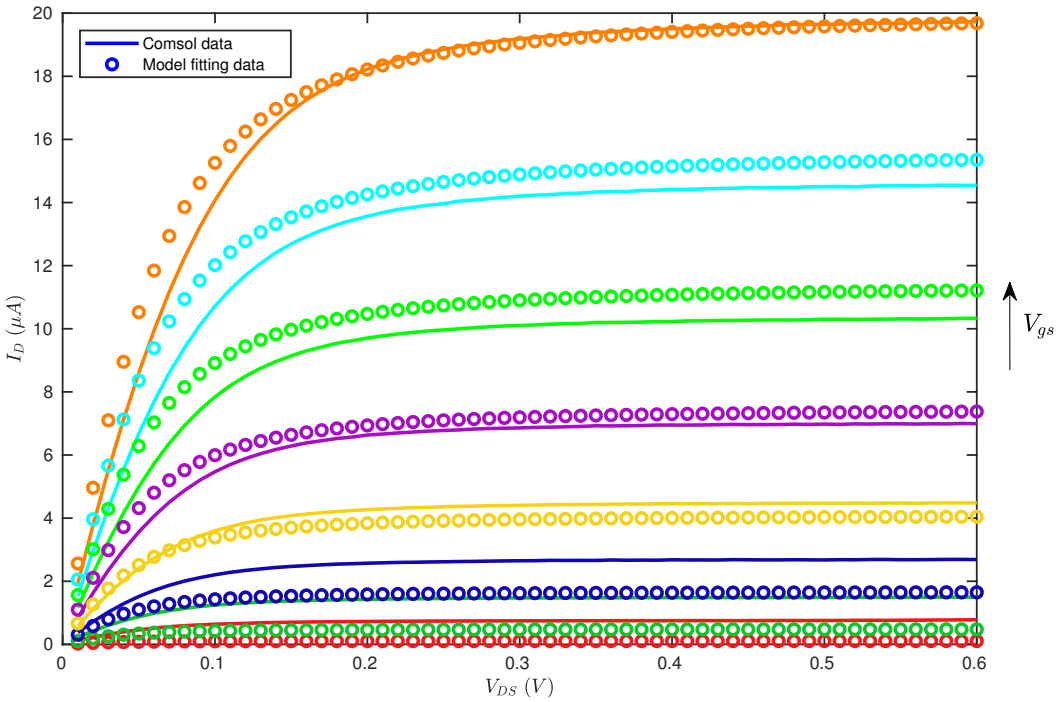

Figure 10. Best model fitting with $L_g = 290$ nm and V_{GS} values from 0.4 V to 0.75 V, with a step size of 0.05 V.

Figure 11 depicts the I_D-V_{GS} curves with the CNTFET in the saturation region, for different values of L_g. In addition, in this case, the experimental results validate the proposed method. Results refer to a number of CNTs in the device $Ncnt = W/s = 100$, supposing a no-border effect.

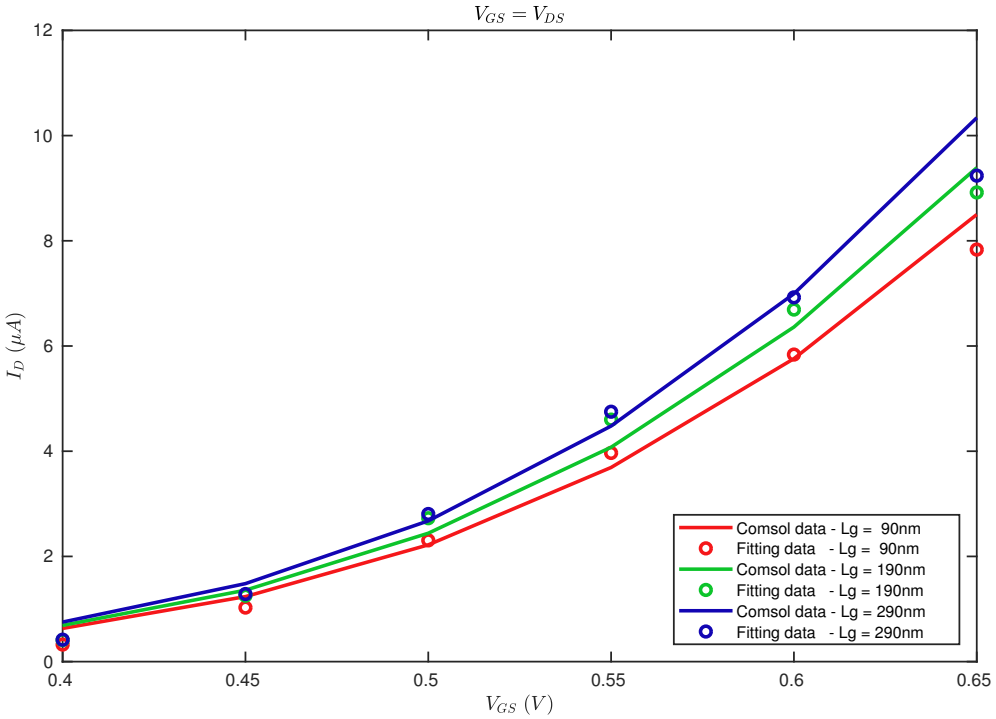

Figure 11. I_D-V_{GS} curves for different values of L_g and $V_{GS} = V_{DS}$ (CNTFET in the saturation region).

As a result, Table 4 reports the values obtained for the fitting parameters of the customized virtual source CNTFET SW model. These values can be used in the Verilog-A model description to develop a SPICE representation of the device.

Table 4. Fitting parameters values for the customized virtual source CNTFET SW model, for three different channel lengths.

Parameter	$L_g = 90$ nm	$L_g = 190$ nm	$L_g = 290$ nm
C_{inv} (fF/µm)	0.761	1.571	2.206
μ ($cm^2V^{-1}s^{-1}$)	1100	1416	1554
V_t (V)	0.549	0.564	0.543
SS (mV/dec)	100	100	100
DIBL (V/V)	0.760	0.787	0.751
R_S (kΩ)	0.554	8.135	0.479
v_{xo} (cm/s)	1.030	5.937	0.427
c_{qa} (fF/µm)	0.022	0.027	0.012
c_{qb} (fF/µm)	0.011	0.006	0.034

It is worth noting that this framework could be potentially applied to fit other device geometries and materials: starting from the known VS-CNTFET model, the user must provide, as an input of the framework, the experimental data derived from full-wave modeling of the specific architecture by using the developed finite element solver (based on the combination of COMSOL Multiphysics and MATLAB), and modify the list of geometrical and physical input parameters (Table 1) according to this architecture. Then, the method should automatically converge to the fitting parameters, in order to

obtain the SPICE representation of the device. Future works are focused on exploring this framework flexibility for new designs and manufacturing nanotechnologies, e.g., silicon nanowires.

5. Conclusions

A compact methodology for the model customization and device parameters extraction of CNTFETs has been proposed. Given the manufacturing technology as well the geometrical data of a custom device architecture, the physical constitutive relations of the CNT channel active region are derived. 3D full-wave simulations of the CNTFET prototype are then performed by means of the COMSOL solver. As a key development, a virtual-source CNTFET single tube model has then been customized, in order to fit it to the COMSOL simulation results. Finally, physical and non-physical parameters for the modified virtual-source CNTFET model have been extracted from the simulation results using a data fitting technique based on the robust simulated annealing algorithm. Additionally, a Verilog-A model description suitable for analog circuit design has been obtained.

Author Contributions: Conceptualization, D.M., P.C., C.T., and L.P.; Data curation, L.F. and N.P.; Formal analysis, L.F. and N.P.; Funding acquisition, L.P.; Methodology, L.F. and N.P.; Project administration, L.P.; Software, L.F., D.M., and N.P.; Supervision, C.T. and L.P.; Validation, L.F.; Visualization, L.F., N.P., P.C., and L.P.; Writing—original draft, L.F., N.P., P.C., G.B., C.T., and L.P.; Writing—review and editing, L.F., N.P., P.C., G.B., C.T., G.D., and L.P. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by the European Project "NANO components for electronic SMART wireless circuits and systems (NANOSMART)", H2020—ICT-07-2018-RIA, n. 825430.

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

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