electronics

MDPI

Article

A High-Gain CNTFET-Based LNA Developed Using a Compact Design-Oriented Device Model

Paolo Crippa [1,*,†], Giorgio Biagetti [1,†], Claudio Turchetti [1,†], Laura Falaschetti [1], Davide Mencarelli [1], George Deligeorgis [2] and Luca Pierantoni [1]

[1] Department of Information Engineering, Università Politecnica delle Marche, 60131 Ancona, Italy; g.biagetti@univpm.it (G.B.); c.turchetti@univpm.it (C.T.); l.falaschetti@univpm.it (L.F.); d.mencarelli@univpm.it (D.M.); l.pierantoni@univpm.it (L.P.)

[2] Microelectronics Research Group (MRG), Institute of Electronic Structure and Laser (IESL), Foundation for Research & Technology Hellas (FORTH), 70013 Crete, Greece; deligeo@physics.uoc.gr

* Correspondence: p.crippa@univpm.it; Tel.: +39-071-220-4541

† These authors contributed equally to this work.

Abstract: Recently, carbon nanotube field-effect transistors (CNTFETs) have attracted wide attention as promising candidates for components in the next generation of electronic devices. In particular CNTFET-based RF devices and circuits show superior performance to those built with silicon FETs since they are able to obtain higher power-gain and cut-off frequency at lower power dissipation. The aim of this paper is to present a compact, design-oriented model of CNTFETs that is able to ease the development of a complete amplifier. As a case study, the detailed design of a high-gain CNTFET-based broadband inductorless LNA is presented.

Keywords: carbon nanotube; CNTFET; low-noise amplifier; LNA; compact model

Citation: Crippa, P.; Biagetti, G.; Turchetti, C.; Falaschetti, L.; Mencarelli, D.; Deligeorgis, G.; Pierantoni, L. A High-Gain CNTFET-Based LNA Developed Using a Compact Design-Oriented Device Model. *Electronics* **2021**, *10*, 2835. https://doi.org/10.3390/electronics10222835

Academic Editors: Andrea Boni and Michele Caselli

Received: 30 October 2021
Accepted: 15 November 2021
Published: 18 November 2021

1. Introduction

Carbon nanotube field-effect transistors (CNTFETs) have demonstrated the ability to be suitable for mixed-signal and RF application, with respect to both conventional bulk semiconductors and 2-D materials, such as graphene [1–6]. This is due to the fact that the 1-D transport in carbon nanotubes (CNTs) leads not only to a low scattering rate and high current-carrying capability but also to a linear I_D vs. V_{GS} transcharacteristic under some conditions [7–9]. This I–V behavior could be considered an advantage in future mobile communication systems where increasingly complex modulation techniques are expected to be used [10].

In particular, RF systems performance mainly depends on their frontend circuit components, such as the low-noise amplifier (LNA), high power amplifier (HPA), single-pole-double-throw (SPDT) switch, oscillator, and mixer. The design of these building blocks is usually implemented through circuit simulators that use compact models representing the actual devices of a given technology. Thus, the need for compact models is of paramount importance for analog RF design where the requirements are quite stringent since the models must accurately describe typically nonlinear devices over a wide range of frequencies, biases, and temperatures.

On the one hand, the device model should be sophisticated enough to take into account the device behavior in different working regions. In particular, the design of RF frontends, including LNAs and HPAs, requires the accurate prediction of (i) the small-signal behavior (that must also include noise) for which the first derivative of the currents and charges with respect to terminal voltages must be correctly modeled, and (ii) large-signal time-domain behavior (along with phase noise) and nonlinear distortion for which an accurate modeling of currents and charges up to at least the fifth-order derivatives is needed.

On the other hand, the device model should be compact and simple enough in order to allow reasonable circuit simulation times. As a consequence, the physical relationships

describing the device behavior must be as simple as possible, e.g., distributed regions of the device have to be represented by lumped elements, and complicated physical effects have to be expressed through simple and explicit analytical solutions [11,12].

Several models have been proposed in the literature that try to approximate the real behavior of the CNTFET device, maintaining their mathematical and computational complexity as low as possible [13–21].

The goal of this paper is to develop a compact and design-oriented device model that is able to describe the device behavior with sufficient details so as to ease the implementation of the main RF building blocks, such as LNA, HPA, and SPDT switch.

Nowadays, the increasing demand for wireless communication systems for broadband, multi-band, and multi-standard receivers makes the bandwidth a critical issue in the design of LNAs [22–28]. Large bandwidth systems exhibit desirable advantages, such as large transmission channel capacity, less multipath fading effect, and easier material penetration. As the first stage of a receiver system, the LNA should have very low noise and provide reasonable voltage gain over the wide band of interest so that the total noise of the receiving chain can be suppressed. In addition, wideband input matching and high linearity also need to be guaranteed. Furthermore, low power consumption and small die area can increase the battery life and decrease the chip cost [29].

Usually, voltage-mode LNAs have many drawbacks, such as limited bandwidth, the need for a high supply and the requirement of a current-to-voltage conversion stage due to the existence of high-impedance nodes. Current-mode LNAs have many intrinsic advantages over voltage-mode counterparts, including low supply voltage requirements, wide bandwidth, tunable input impedances, and high slew rates. In recent years, several articles about current-mode wideband LNAs in standard CMOS technology have been reported [28,30–36].

According to the input matching and noise characteristics of the circuit, LNA has two typical architectures, common source (CS) and common gate (CG) topology. The wideband input matching is provided by the CG topology, but it has a high noise figure (NF) [28]. In the CG LNA topology, most input and/or output matching is achieved by employing inductors and capacitors to achieve broadband matching, which greatly increases the chip area and cost. The advantage of CS topology can get higher gain, but compromises need to be made between gain and broadband input matching. In order to reduce the contradiction between the gain of CS topology and the input matching bandwidth, a resistive feedback technique is usually used to obtain considerable gain and wideband input matching.

With these considerations in mind, we chose to apply our previously developed compact CNTFET model [37] to the design of a cascode LNA. The model was derived from electromagnetic and quantistic simulations that are supposed to mimic the actual technology that will be used for circuit manufacturing, and although it has not yet been validated experimentally, it should be a good starting point to estimate the performance this technology could achieve. The cascode architecture was chosen because it combines the high gain and low NF of a CS topology with the higher operating frequencies of the CG topology and is thus of interest in RF applications.

This paper is organized as follows. In Section 2, the extrinsic CNTFET model comprising noise sources is presented. In Section 3, the simplified DC CNTFET model is described. In Section 4, the proposed device model was applied to the design flow of an LNA. Section 5 reports some simulation results and comparisons. Finally, Section 6 concludes this work.

2. CNTFET Extrinsic Noise Model

As a first step to designing a low-noise amplifier, a suitable model of the noise sources within the employed active devices is necessary. We assume that noise can be modeled by adding stochastic current sources in parallel to the main small-signal elements of the standard FET equivalent circuit and to the contact resistances [25], as shown in Figure 1, which is valid in the saturation region of the transistor.

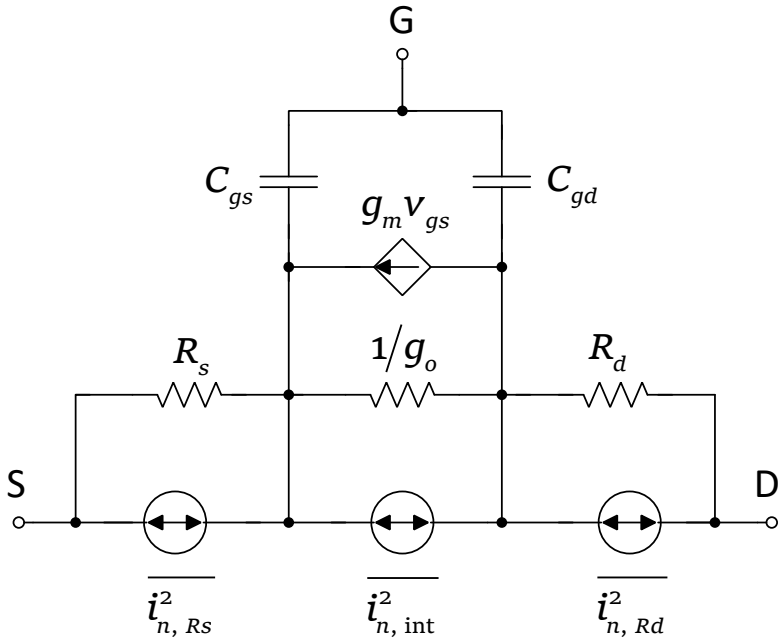

Figure 1. CNTFET noise model in the saturation region.

Here, g_m and g_o are the intrinsic FET transconductance and output conductance, respectively, R_d and R_s represent the channel resistance at the drain and source terminals, respectively, while C_gs and C_gd model the capacitive effects of the gate.

The noise sources $\overline{i^2_{\mathrm{n},x}}$, where x can denote the noise associated with the source (Rs), drain (Rd) or the intrinsic device (int), can be assumed to have a power spectral density proportional to the transistor drain current I_D:

$$\overline{i^2_{\mathrm{n},x}} = 2\,q\,I_\mathrm{D}\,F_x \tag{1}$$

where q is the elementary charge and F_x is the appropriate Fano factor. According to [25], it is common to assume $F_\mathrm{Rs} = F_\mathrm{Rd} = 0.3$ if the contact resistances are mostly due to the doped nanotube extensions, while F_int might depend both on technological details of the nanotubes and transistor bias. However, from [38], F_int can be assumed to be almost constant and smaller than 0.1 for a wide range of typical bias currents. For simplicity, we will conservatively assume $F_\mathrm{int} = 0.1$ in our simulations.

From that, we aim to derive a simplified extrinsic model composed of just the transconductance element, the output conductance, and a single noise current source, all in parallel. From a rapid inspection of the equivalent circuit reported in Figure 1, the extrinsic transconductance g^*_m can be expressed as:

$$g^*_\mathrm{m} = \frac{g_\mathrm{m}}{1 + g_\mathrm{m} \cdot R_\mathrm{s}} \tag{2}$$

and the extrinsic output conductance g^*_o can also be expressed as:

$$g^*_\mathrm{o} = \frac{g_\mathrm{o}}{1 + g_\mathrm{m} \cdot R_\mathrm{s} + g_\mathrm{o} \cdot (R_\mathrm{s} + R_\mathrm{d})} \tag{3}$$

where obviously both of them can be approximated by g_m and g_o, respectively, when the contact resistances R_s and R_d are vanishing.

The total noise density $\overline{i^2_{\mathrm{n,TOT}}}$ in the saturation region can be calculated as below:

$$\overline{i^2_{\mathrm{n,TOT}}} = \left[\frac{(g_\mathrm{m}+g_\mathrm{o})\cdot R_\mathrm{s}}{1+g_\mathrm{m}\cdot R_\mathrm{s}+g_\mathrm{o}\cdot(R_\mathrm{s}+R_\mathrm{d})}\right]^2 \cdot \overline{i^2_{\mathrm{n,Rs}}} + \left[\frac{1}{1+g_\mathrm{m}\cdot R_\mathrm{s}+g_\mathrm{o}\cdot(R_\mathrm{s}+R_\mathrm{d})}\right]^2 \cdot \overline{i^2_{\mathrm{n,int}}} + \left[\frac{g_\mathrm{o}\cdot R_\mathrm{d}}{1+g_\mathrm{m}\cdot R_\mathrm{s}+g_\mathrm{o}\cdot(R_\mathrm{s}+R_\mathrm{d})}\right]^2 \cdot \overline{i^2_{\mathrm{n,Rd}}} \quad (4)$$

which is in parallel to the equivalent output conductance g^*_o.

For completeness, the CNTFET simplified extrinsic model with noise sources in the triode region can be derived similarly. The small-signal equivalent circuit is reported in Figure 2, and the total noise in the triode region can be calculated as below:

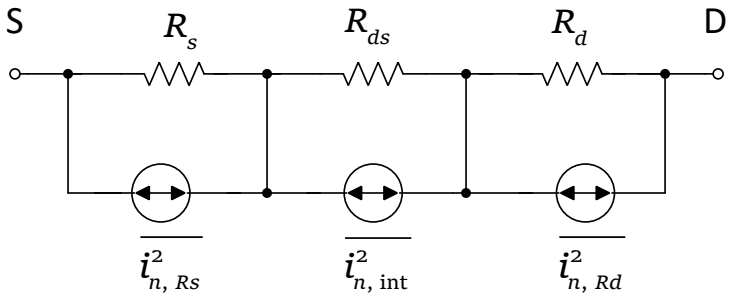

Figure 2. CNTFET noise model in triode region.

$$\overline{i^2_{\mathrm{n,TOT}}} = \left[\frac{R_\mathrm{s}}{R_\mathrm{s}+R_\mathrm{ds}+R_\mathrm{d}}\right]^2 \cdot \overline{i^2_{\mathrm{n,Rs}}} + \left[\frac{R_\mathrm{ds}}{R_\mathrm{s}+R_\mathrm{ds}+R_\mathrm{d}}\right]^2 \cdot \overline{i^2_{\mathrm{n,int}}} + \left[\frac{R_\mathrm{d}}{R_\mathrm{s}+R_\mathrm{ds}+R_\mathrm{d}}\right]^2 \cdot \overline{i^2_{\mathrm{n,Rd}}} \quad (5)$$

where R_ds is the on-state resistance of the transistor in the triode region.

Having derived this simplified extrinsic model, in the following, we will always refer to the extrinsic parameters when talking about g_m and g_o, without encumbering the notation with the asterisk (g^*) symbol.

3. DC CNTFET Simplified Model

In order to simplify the design process of the amplifier, a compact, designer-friendly model of the behavior of the drain current in a CNTFET that is suitable for estimating operating points can also be useful.

To develop such a model, it is important to understand the differences in behavior between a conventional MOSFET and a CNTFET of the type analyzed in [37], which, unlike many other studied structures, exhibits a drain current relationship with respect to biasing voltages that is almost exactly a separable function of the gate and drain voltages. This can be seen in Figure 3, which shows the input and output characteristics on a normalized vertical axis (i.e., individual current curves had been divided by their mean value).

For what regards the input characteristics, it can be seen that the drain current is almost linearly dependent on the gate overdrive voltage above the threshold voltage and that the curve shape does not depend at all on drain voltage. On the other hand, for what concerns the CNTFET output characteristics, there is a very weak, and negligible, dependence of their shape on the gate voltage, but unlike conventional MOSFETs, the saturation region, where the characteristic becomes almost linear, can be assumed to start from a fixed voltage that it is not bound to the gate overdrive voltage, thus allowing a great simplification of both the empirical model and of the design procedure.

It is thus reasonable to employ a simple empirical model with separated variables, such as:

$$I_\mathrm{D} = g_\mathrm{m}\, f_\mathrm{G}(V_\mathrm{GS}-V_\mathrm{TH})\, f_\mathrm{D}(V_\mathrm{DS}/V_\mathrm{p})\,(1+\lambda\, V_\mathrm{DS}) \quad (6)$$

where f_G should mimic the shape on the left panel of Figure 3, and f_D that on the right panel.

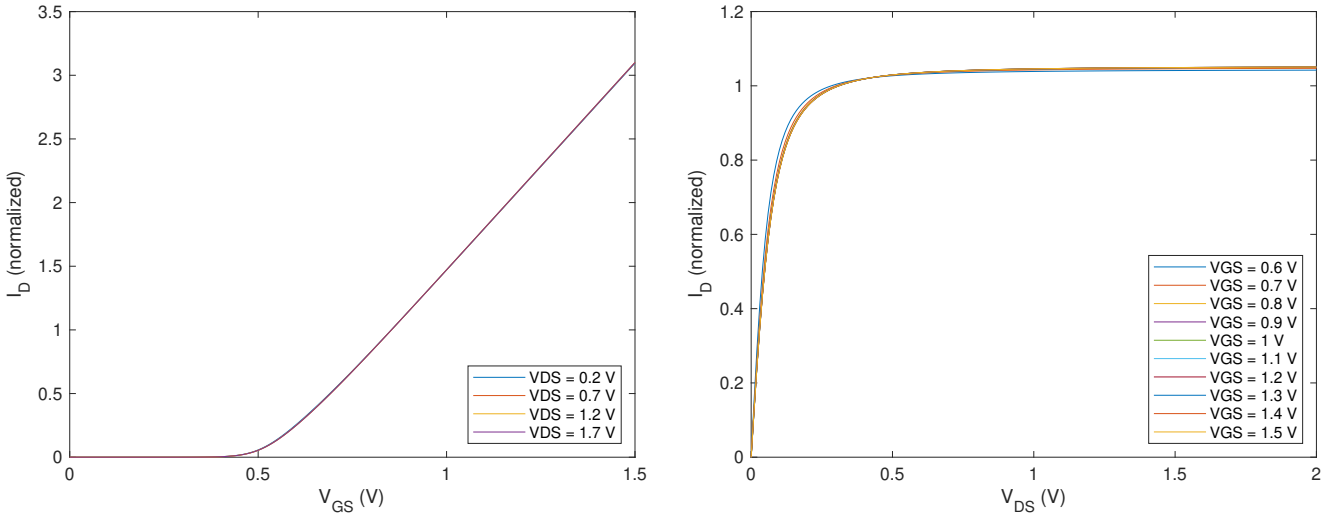

Figure 3. Example input (**left panel**) and output (**right panel**) normalized characteristics of a CNTFET with a channel width $W = 1$ µm and a channel length $L = 90$ nm. The curves are predicted by the model developed in [37], for different biasing voltages. Normalization was performed by dividing each individual curve by its mean value.

If maximum simplicity is sought, and the circuit only operates well above threshold, a simple, piecewise linear model for f_{G} might suffice, such as:

$$f_{\mathrm{G}}(v) = \min(0, v) \tag{7}$$

otherwise, a slightly more smoothed version can better approximate sub-threshold and near-threshold behavior:

$$f_{\mathrm{G}}(v) = \begin{cases} V_\sigma \log\left(1 + \exp(\frac{v}{V_\sigma})\right) & v > 0 \\ V_\sigma \log\left(1 + \exp(\frac{v}{k\,V_\sigma})\right) & v < 0 \end{cases} \tag{8}$$

where V_σ is a parameter that determines the width of the smoothed transition region, and k is a parameter that can be used to adjust the sub-threshold transconductance. It can be noted that Equation (7) is the limit of Equation (8) as $V_\sigma \to 0$, and that $\partial f_{\mathrm{G}}(v)/\partial v|_{v \gg 0} = 1$ so that g_{m} retains its normal meaning.

On the other hand, $f_{\mathrm{D}}(x)$ can be assumed as a saturating power function to describe the dependence on V_{DS}, such as:

$$f_{\mathrm{D}}(x) = \begin{cases} (n\,x - x^n)/(n-1) & 0 < x \leq 1 \\ \\ 1 & x > 1 \end{cases} \tag{9}$$

which satisfies the properties $\forall n \neq 1$, $f_{\mathrm{D}}(0) = 0$, $f_{\mathrm{D}}(1) = 1$, $\partial f_{\mathrm{D}}(x)/\partial x|_{x=1} = 0$.

We thus have a total of seven fitting parameters: g_{m} and V_{TH} are the slope and threshold voltage of the input characteristics, respectively, while V_σ controls the near-threshold behavior and k the sub-threshold transconductance. For the output characteristics, V_{p} is the equivalent of the "pinch-off" voltage that denotes the starting of the saturation region, λ defines the output resistance ($g_{\mathrm{o}} \simeq \lambda I_{\mathrm{D}}$), and the exponent n controls the "steepness" of the transition between the triode and saturation regions.

These parameters can be fitted to match the simplified model to the full-fledged simulation, as shown in Figure 4 for a $W = 1$ µm CNTFET (100 nanotubes).

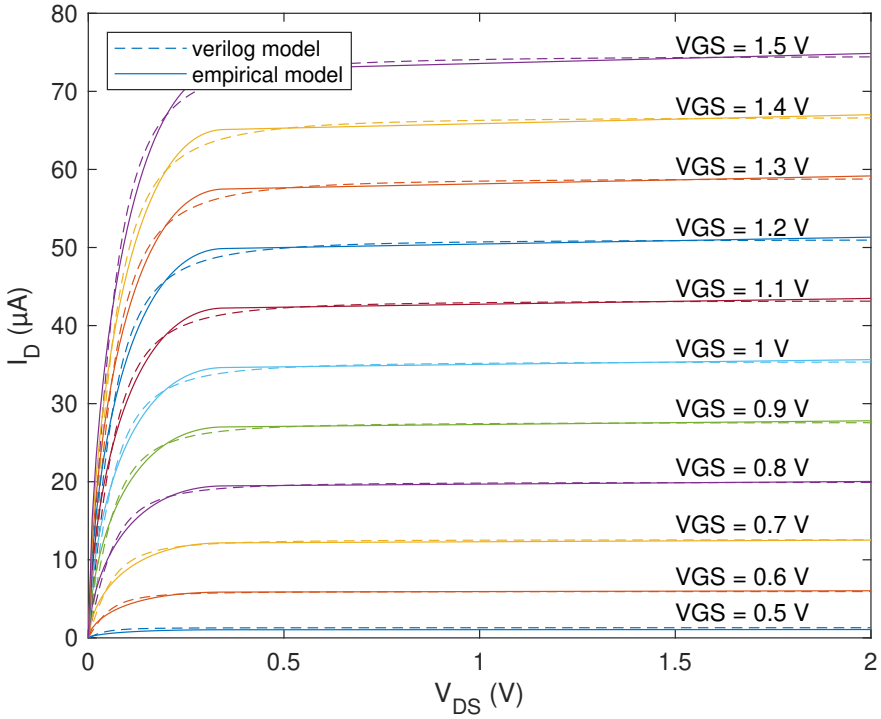

Figure 4. Fitting of the simplified DC model to the full-fledged Verilog-A model. $g_{\mathrm{m}} = 75.76\,\mu\mathrm{S}$, $V_{\mathrm{TH}} = 0.546\,\mathrm{V}$, $V_{\sigma} = 63.8\,\mathrm{mV}$, $\lambda = 0.0178\,\mathrm{V}^{-1}$, $V_{\mathrm{p}} = 0.344\,\mathrm{V}$, $n = 0.7$, $k = 0.5$.

4. LNA Design

The above model was applied to the design of an LNA. The architecture we chose is based on the widely-adopted cascode configuration since it can provide a good noise figure, modified by replacing the common-gate stage with a gm-boosting architecture. The schematic is shown in Figure 5.

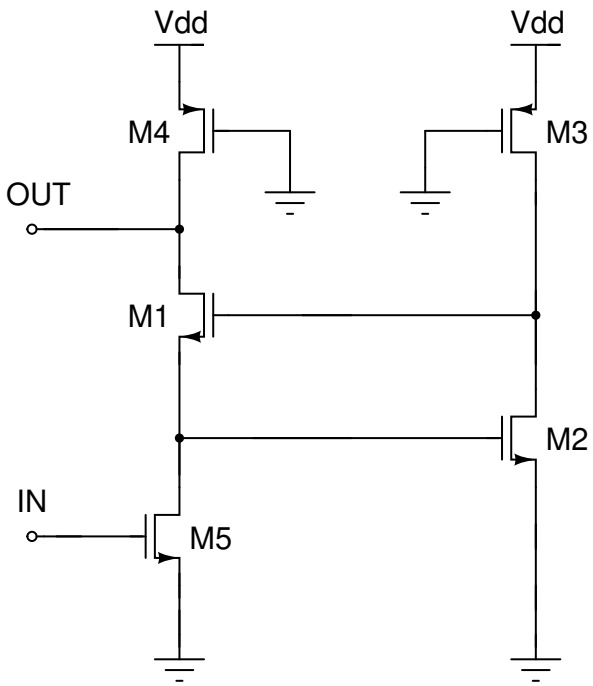

Figure 5. LNA schematic.

The gm-boosting effect is provided by the secondary amplifier composed of M_2 and M_3. Together, they actively provide the gate voltage to the common-gate stage M_1 so

that its source is kept at a nearly constant voltage. This architecture indeed provides a much lower input impedance than a simple transistor, and that essentially cancels the Miller effect on the drain-gate capacitance of M_5, enlarging the operational frequency of the amplifier.

By simple circuit inspection, it is possible to compute that the resistance seen from the drain of M_5 is indeed (neglecting the output conductance of M_1):

$$R_{\mathrm{GB}} \simeq \frac{1}{g_{\mathrm{m1}}} \frac{1}{1+|A_{\mathrm{v2}}|} \tag{10}$$

where A_{v2} is the gain of the secondary amplifier.

$$A_{\mathrm{v2}} = \frac{-g_{\mathrm{m2}}}{g_{\mathrm{o2}}+g_{\mathrm{o3}}} \simeq \frac{-1}{2\,\lambda\,(V_{\mathrm{G2}}-V_{\mathrm{TH}})} \tag{11}$$

so that the voltage gain of the first stage (M_5) is very low:

$$A_{\mathrm{v1}} = -g_{\mathrm{m5}}\,R_{\mathrm{GB}} \simeq -\frac{g_{\mathrm{m5}}}{g_{\mathrm{m1}}} \frac{1}{1+|A_{\mathrm{v2}}|} \tag{12}$$

and $|A_{\mathrm{v1}}| \ll 1$ provided that g_{m5} and g_{m1} are comparable (as they should be) being the two transistors M_5 and M_1 biased with the same current. This way, the input capacitance of the amplifier reduces to:

$$C_{\mathrm{in}} = C_{\mathrm{gs5}} + C_{\mathrm{gd5}}\,(1-A_{\mathrm{v1}}) \simeq C_{\mathrm{gs5}} + C_{\mathrm{gd5}} \tag{13}$$

instead of $C_{\mathrm{gs5}} + C_{\mathrm{gd5}}(1+g_{\mathrm{m5}}/g_{\mathrm{m1}})$ we would have had without the gm-boosting stage.

Back to the complete amplifier, its gain can be computed with reference to its small-signal equivalent circuit shown in Figure 6. There, for notational simplicity, we imply that g_{o4} also includes the output load conductance (and so will be much higher than the output conductances of the other transistors).

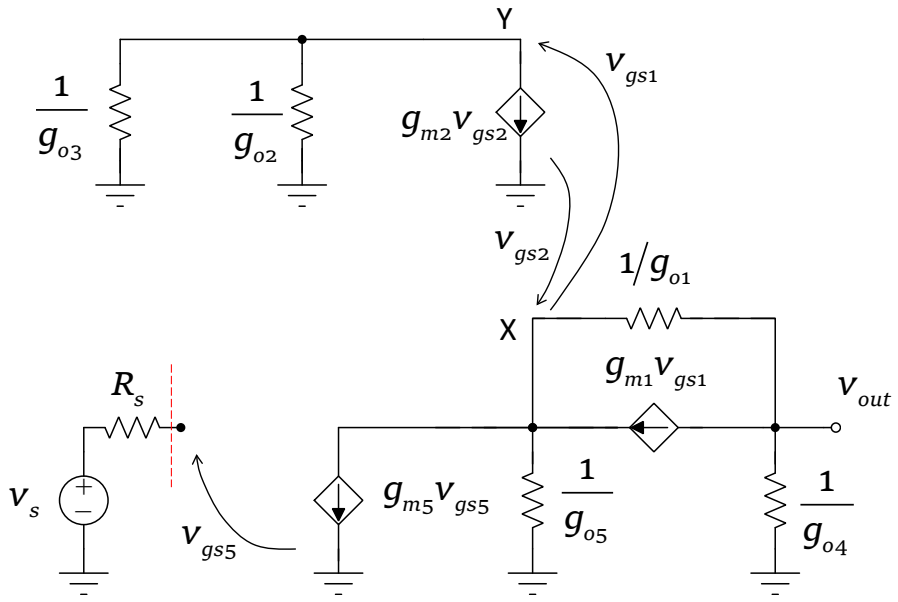

Figure 6. LNA equivalent circuit.

The overall voltage gain is then:

$$A_{\mathrm{v}} = -\frac{g_{\mathrm{m5}}\cdot[g_{\mathrm{o1}}(g_{\mathrm{o2}}+g_{\mathrm{o3}})+g_{\mathrm{m1}}(g_{\mathrm{m2}}+g_{\mathrm{o2}}+g_{\mathrm{o3}})]}{(g_{\mathrm{o1}}\cdot g_{\mathrm{o5}}+g_{\mathrm{o4}}\cdot g_{\mathrm{o5}}+g_{\mathrm{o1}}\cdot g_{\mathrm{o4}})\cdot(g_{\mathrm{o2}}+g_{\mathrm{o3}})+g_{\mathrm{m1}}\cdot g_{\mathrm{o4}}\cdot(g_{\mathrm{m2}}+g_{\mathrm{o2}}+g_{\mathrm{o3}})} \tag{14}$$

and, considering the output conductances to be negligible with respect to transconductances, the voltage gain simplifies as follows:

$$A_{\mathrm{v}} \simeq -\frac{g_{\mathrm{m5}}}{g_{\mathrm{o4}}} \tag{15}$$

4.1. Amplifier Noise Evaluation

Considering all the CNTFET noise contributions, we have the following equations:

$$(g_{\mathrm{o2}} + g_{\mathrm{o3}}) \cdot v_{\mathrm{y}} = -g_{\mathrm{m2}} \cdot v_{\mathrm{x}} - i_{\mathrm{n2}} - i_{\mathrm{n3}} \tag{16}$$

$$g_{\mathrm{o4}} \cdot v_{\mathrm{out}} + i_{\mathrm{n4}} = -g_{\mathrm{m1}} \cdot (v_{\mathrm{y}} - v_{\mathrm{x}}) - g_{\mathrm{o1}} \cdot (v_{\mathrm{out}} - v_{\mathrm{x}}) - i_{\mathrm{n1}} \tag{17}$$

$$g_{\mathrm{o5}} \cdot v_{\mathrm{x}} + i_{\mathrm{n5}} = -g_{\mathrm{o4}} \cdot v_{\mathrm{out}} - i_{\mathrm{n4}} \tag{18}$$

where v_{x} and v_{y} are the voltages at the nodes X and Y of the equivalent circuit Figure 6, respectively.

By solving (16)–(18) and considering the output conductances g_{o1}, g_{o2}, g_{o3}, g_{o5} vanishing with respect to the CNTFET transconductances g_{m}, the five CNTFET noise contributions to the output voltage v_{out} result in:

$$v_{\mathrm{out}}^{(\mathrm{n})} \simeq -\frac{(g_{\mathrm{o2}} + g_{\mathrm{o3}}) \cdot g_{\mathrm{o5}}}{g_{\mathrm{m1}} \cdot g_{\mathrm{m2}} \cdot g_{\mathrm{o4}}} \cdot i_{\mathrm{n1}} + \frac{g_{\mathrm{o5}}}{g_{\mathrm{m2}} \cdot g_{\mathrm{o4}}} \cdot i_{\mathrm{n2}} + \frac{g_{\mathrm{o5}}}{g_{\mathrm{m2}} \cdot g_{\mathrm{o4}}} \cdot i_{\mathrm{n3}} - \frac{1}{g_{\mathrm{o4}}} \cdot i_{\mathrm{n4}} - \frac{1}{g_{\mathrm{o4}}} \cdot i_{\mathrm{n5}} \tag{19}$$

4.2. DC Bias Design Procedure and Optimization

Due to the separability property of the functional dependence of the drain current with respect to the gate and drain voltages, biasing of the circuit is quite straightforward, and the overall small-signal gain only depends on the input transistor and load, as shown in (15).

Nevertheless, the noise performance is indeed influenced by the bias currents and voltages, and so the design can be tailored to optimize such a performance.

In particular, from Equation (19), it is apparent that only M_4 and M_5 make a significant contribution to the output noise, with their noise currents directly flowing into the output conductance (g_{o4}). Since the equivalent noise current power spectral density $\overline{i_{\mathrm{n}}^2}$ of a single transistor is proportional to its drain current:

$$\overline{i_{\mathrm{n}}^2} \propto I_{\mathrm{D}} \tag{20}$$

while its transconductance g_{m} also depends on gate biasing:

$$g_{\mathrm{m}} \simeq \frac{I_{\mathrm{D}}}{V_{\mathrm{GS}} - V_{\mathrm{TH}}} \tag{21}$$

it is possible to optimize M_5 for noise performance by maximizing its g_{m}, while nothing, unfortunately, can be done for the noise added by M_4.

The noise factor of the input stage, a CS configuration, can thus be computed as:

$$F = \frac{S_{\mathrm{i}}/N_{\mathrm{i}}}{S_{\mathrm{o}}/N_{\mathrm{o}}} = \frac{\overline{v_{\mathrm{i}}^2}/\overline{v_{\mathrm{n}}^2}}{\overline{g_{\mathrm{m}}^2\, v_{\mathrm{i}}^2}/(\overline{g_{\mathrm{m}}^2\, v_{\mathrm{n}}^2} + \overline{i_{\mathrm{n}}^2})} = 1 + \frac{\overline{i_{\mathrm{n}}^2}}{\overline{g_{\mathrm{m}}^2\, v_{\mathrm{n}}^2}} \tag{22}$$

where S_{i} and S_{o} are the power spectral densities of the input voltage signal (v_{i}) and output current signal ($g_{\mathrm{m}}\, v_{\mathrm{i}}$), respectively, and similarly N_{i} and N_{o} for the input noise (v_{n}) and added output noise (i_{n}). Due to Equations (20) and (21), the above Equation (22) becomes:

$$F - 1 \propto \frac{(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2}{I_{\mathrm{D}}} \tag{23}$$

so that it is best to bias the transistor with the lowest possible overdrive voltage, provided that sufficient linearity is retained. Of course, this implies a trade-off with bandwidth, as lower overdrive voltages require larger transistors to sustain the desired drain current.

With these considerations in mind, it is possible to proceed with the design optimization after having defined a few constraints that are needed on the node voltages to ensure all transistors are biased in their saturation region. To aid optimization, normalized node voltages are used, i.e., if a node n must have a voltage V_n constrained so that $V_{\mathrm{L}n} < V_n < V_{\mathrm{H}n}$, then we pose $x_n = (V_n - V_{\mathrm{L}n})/(V_{\mathrm{H}n} - V_{\mathrm{L}n})$, and the optimizer can (theoretically) explore the whole unitary hypercube $0 \leq x_n \leq 1$.

To do so, the currents in the left and right branches, I_1 and I_2, respectively, must also be fixed, but those are usually determined by system-level considerations on the maximum power dissipation of the device. From a noise perspective, the higher the currents, the better. We thus chose to use $I_1 = 7\,\mathrm{mA}$ and $I_2 = 2\,\mathrm{mA}$, since the right branch transistors do not contribute much to the total noise of the LNA.

To minimize noise, from Equation (23), V_{G5} should be as low as possible, which also has the effect of maximizing the transistor M_5 transconductance and hence the gain of the whole amplifier. We thus fixed $x_{\mathrm{G5}} = 0.1$ to allow for some signal excursion without losing linearity. The other transistors can be designed to keep their total size as small as possible, aiding in the frequency response. Since $g_{\mathrm{m}} \propto W$, transistors widths W can easily be computed from Equation (21) once the currents and voltages are known, and so a numeric optimizer can be employed. Minimization of the total gate area of the amplifier thus leads to the results shown in Table 1, where the search for internal node bias has been further constrained to the range between 10% and 90% of the possible swing.

Table 1. LNA biasing constraints and optimized values. $V_{\mathrm{L}n}$ is the minimum allowed node voltage, and $V_{\mathrm{H}n}$ is the maximum. The last two columns report the final optimized node voltage as a percentage of the allowed swing (x_n) and in volts (V_n).

Node n	$V_{\mathrm{L}n}$	$V_{\mathrm{DD}} - V_{\mathrm{H}n}$	x_n (%)	V_n (V)
D1	$V_{\mathrm{G2}} + V_{\mathrm{p}}$	V_{p}	50	1.3559
G1	$V_{\mathrm{G2}} + V_{\mathrm{TH}}$	V_{p}	90	1.6302
G2	V_{TH}	$V_{\mathrm{p}} + V_{\mathrm{TH}}$	30	0.7118
G3	0	V_{TH}	0	0.0000
G4	0	V_{TH}	0	0.0000
G5	V_{TH}	0	10	0.6716

It may be worth noticing that the optimal bias for the gates of M_3 and M_4 turned out to be ground (due to having minimized their widths), which is very convenient as only one bias generator (for the gate of M_5) is needed for best LNA operation. The resulting transistor widths are shown in Table 2.

Table 2. CNTFET sizes as determined by numerical optimization of the LNA.

FET	W (µm)	I_{D} (mA)
M_1	250.6	7
M_2	150.4	2
M_3	19.1	2
M_4	67.0	7
M_5	669.6	7

5. Simulation Results

Extensive simulations have been performed using the complete Verilog-A CNTFET model to ensure that the amplifier, designed with the simplified model, actually performs according to its designed specifications.

As a first test, Figure 7 reports the voltage gain of the amplifier. From the design data reported in Table 2, its nominal value should be around 25.7 dB, and as can be seen, the achieved gain is pretty close, with a -3 dB bandwidth of about 2.5 GHz.

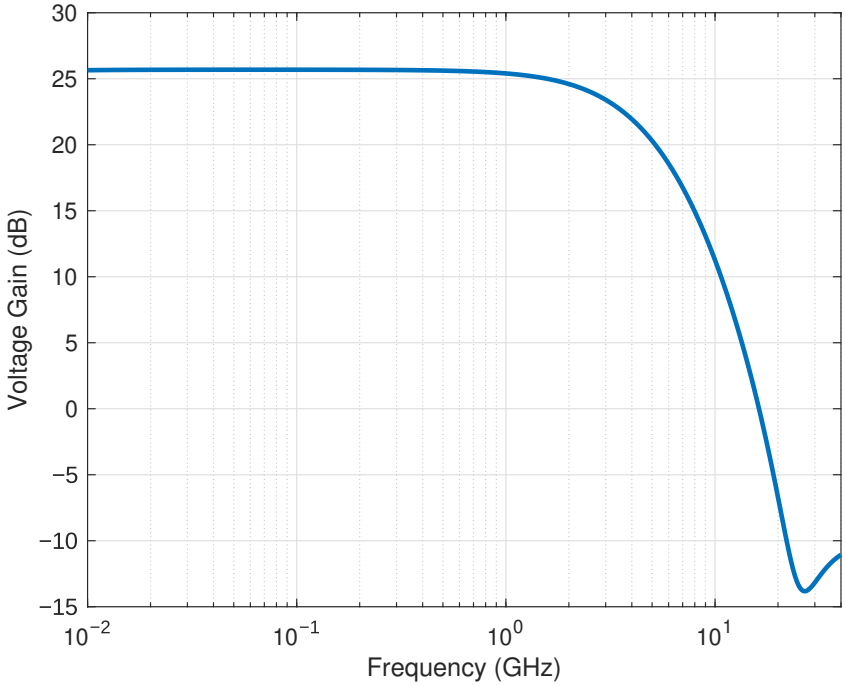

Figure 7. Overall LNA voltage gain with a 500 Ω load.

The noise factor depends, of course, on the parameters used for the noise model, for which, unfortunately, we could not find enough experimental data to validate the value we used in our model and on the biasing of the input transistor, as discussed earlier. Nevertheless, with the values reported in the main text, the amplifier achieves around 1 dB of noise figure within the amplifier bandwidth, as shown in Figure 8.

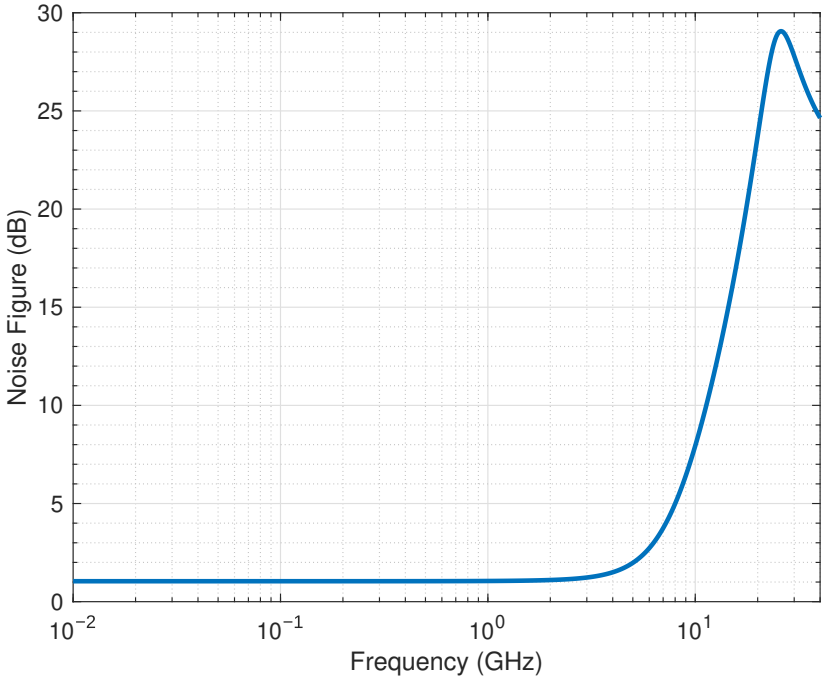

Figure 8. LNA noise factor.

Its linearity is also very good, due to the intrinsically linear input characteristics of the above CNTFET threshold, as demonstrated by the input-referred 1 dB compression point shown in Figure 9, which, considering the high gain of the amplifier, is essentially limited only by the swing of the output node.

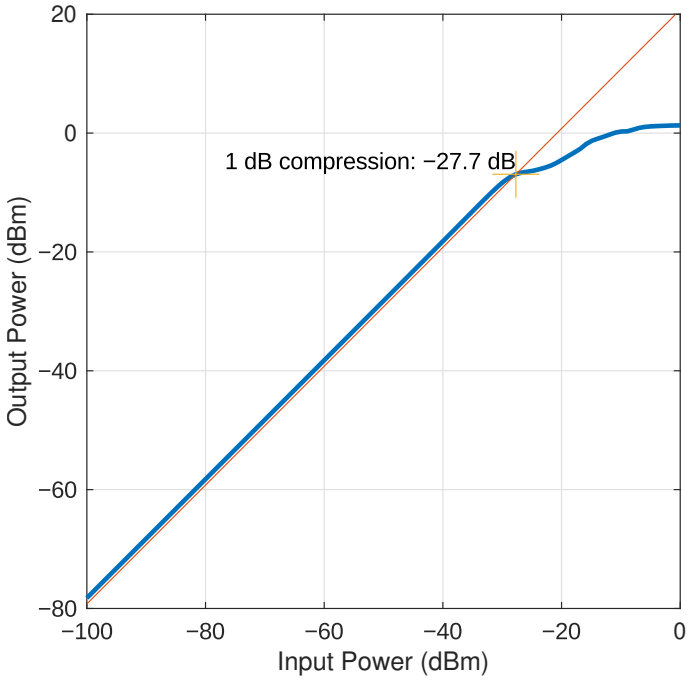

Figure 9. LNA linearity: 1-dB input-referred compression point.

Finally, the stability of the amplifier was also evaluated by a pole-zero analysis, reported in Figure 10, from which it is clear that the amplifier is indeed stable (all poles have negative real parts). It is also clearly visible that the amplifier bandwidth is limited by the pair of complex conjugate poles at around 2.5 GHz.

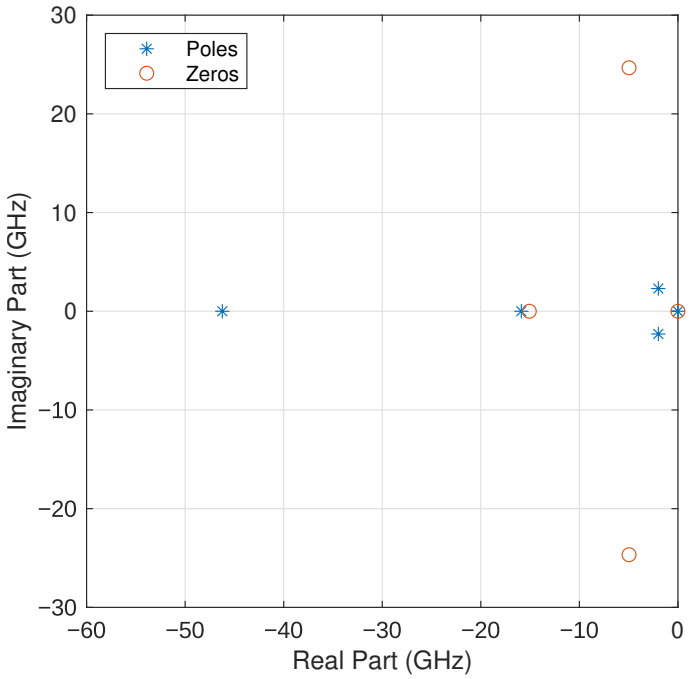

Figure 10. Pole-zero diagram of the amplifier showing LNA stability.

A summary of the achieved performance is shown in Table 3, together with a comparison with those obtained by similar works, also taking into account some results relative to conventional CMOS LNAs, as there are still not many works that focus on LNAs made with CNTFET.

Table 3. Performance comparison of the designed LNA with other works.

Reference	[22]	[23]	[24]	[25]	[26]	[29]	[27]	[28]	This Work
Node	180 nm	180 nm	450 nm	32 nm	65 nm	130 nm	65 nm	130 nm	90 nm
Technology	CMOS	CMOS	CNTFET	CNTFET	CMOS	CMOS	CMOS	CMOS	CNTFET
Data	Sim.	Meas.	Meas.	Sim.	Meas.	Meas.	Sim.	Sim.	Sim.
Bandwidth (GHz)	3–6	1.05–3.05	1–1.2	3–38	1–20	0.1–2.7	0.03–3	0.1–5	0.01–2.5
Power Supply (V)	1.8	1.8	2.5	1.0	1.6	1.2	1.2	1.2	2.0
Power (mW)	15.3	12.6	N/A	16	20.3	1.32	5.7	4.4	18
Gain (dB)	20.14–21	16.9	11	13.7–14.7	12.8	20	11.6	20	25.7
NF (dB)	3.5–3.6	2.6–3.1	8	0.4–1.3	3.3–5.3	4.0	2.7–3.32	3.04–3.97	1.0

In particular, with respect to the two CNTFET LNAs reported in the table, our architecture has the highest gain, which could be obtained without sacrificing bandwidth due to the gm-boosting technique adopted. The high gain also helped in achieving a low NF, of the same order as the best CNTFET LNA reported in the table and at a comparable power dissipation level, and much lower than the CMOS alternatives, due to the intrinsic lower noise of the carbon nanotubes versus conventional transistors.

Of course, due to the relatively young stage of the CNT technology we are designing, and to the fact that the model used was fitted to simulated data, we expect that it might not capture all the details of the manufactured transistor. Actual devices might perform slightly differently and also exhibit parameter device variations, such as device mismatch, that might affect circuit biasing and thus the overall RF performance.

6. Conclusions

In this work, a designer-friendly, simplified model of CNTFET was developed and fitted to previously published data. Its simplicity, stemming from the separability property of the functional dependence of the drain current on the gate and drain voltages, allow direct design and optimization of circuit bias points, as was demonstrated by the designing of a CNTFET LNA. That, coupled with a noise model to optimize the overall noise figure of the amplifier, was then simulated using the full-fledged Verilog-A Stanford model augmented with noise sources. The simulation results show good agreement to the predicted performance, proving the correctness and usefulness of the proposed simplifications. A comparison of the circuit performance was also made with reference to several state-of-the-art architectures found in the literature, encompassing both conventional CMOS technologies and CNTFET circuits, confirming the overall validity of the proposed high-gain LNA design.

Author Contributions: Conceptualization, P.C., G.B., C.T., L.F., D.M., G.D. and L.P.; methodology, P.C., G.B. and C.T.; software, P.C. and G.B.; formal analysis, P.C., G.B., C.T. and L.F.; investigation, P.C., G.B. and C.T.; resources, G.D.; data curation, L.F. and D.M.; writing—original draft preparation, P.C. and G.B.; writing—review and editing, P.C., G.B., C.T., L.F., D.M., G.D. and L.P.; visualization, P.C. and G.B.; supervision, C.T.; project administration, L.P.; funding acquisition, G.D. and L.P.; All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by the European Project "NANO components for electronic SMART wireless circuits and systems (NANOSMART)", H2020—ICT-07-2018-RIA, n. 825430.

Data Availability Statement: No new data were created or analyzed in this study. Data sharing is not applicable to this article.

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

References

1. Moaiyeri, M.H.; Khastoo, N.; Nasiri, M.; Navi, K.; Bagherzadeh, N. An efficient analog-to-digital converter based on carbon nanotube FETs. *J. Low Power Electron.* **2016**, *12*, 150–157. [CrossRef]
2. Zanjani, S.M.A.; Dousti, M.; Dolatshahi, M. Inverter-based, low-power and low-voltage, new mixed-mode Gm-C filter in subthreshold CNTFET technology. *IET Circuits Devices Syst.* **2018**, *12*, 681–688. [CrossRef]
3. Jooq, M.K.Q.; Mir, A.; Mirzakuchaki, S.; Farmani, A. Design and performance analysis of wrap-gate CNTFET-based ring oscillators for IoT applications. *Integration* **2020**, *70*, 116–125. [CrossRef]
4. Schröter, M.; Claus, M.; Hermann, S.; Tittman-Otto, J.; Haferlach, M.; Mothes, S.; Schulz, S. CNTFET-based RF electronics—State-of-the-art and future prospects. In Proceedings of the 2016 IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), Austin, TX, USA, 24–27 January 2016; pp. 97–100.
5. Ramos-Silva, J.N.; Pacheco-Sanchez, A.; Diaz-Albarran, L.M.; Rodriguez-Mendez, L.M.; Enciso-Aguilar, M.A.; Schröter, M.; Ramírez-García, E. High-frequency performance study of CNTFET-based amplifiers. *IEEE Trans. Nanotechnol.* **2020**, *19*, 284–291. [CrossRef]
6. Khaleqi Qaleh Jooq, M.; Bozorgmehr, A.; Mirzakuchaki, S. A low-power delay stage ring VCO based on wrap-gate CNTFET technology for X-band satellite communication applications. *Int. J. Circuit Theory Appl.* **2021**, *49*, 142–158. [CrossRef]
7. Baumgardner, J.E.; Pesetski, A.A.; Murduck, J.M.; Przybysz, J.X.; Adam, J.D.; Zhang, H. Inherent linearity in carbon nanotube field-effect transistors. *Appl. Phys. Lett.* **2007**, *91*, 052107. [CrossRef]
8. Mothes, S.; Claus, M.; Schröter, M. Toward linearity in Schottky barrier CNTFETs. *IEEE Trans. Nanotechnol.* **2015**, *14*, 372–378. [CrossRef]
9. Alam, A.U.; Rogers, C.M.S.; Paydavosi, N.; Holland, K.D.; Ahmed, S.; Vaidyanathan, M. RF linearity potential of carbon-nanotube transistors versus MOSFETs. *IEEE Trans. Nanotechnol.* **2013**, *12*, 340–351. [CrossRef]
10. Weller, K. Mobile broadband system evolution and RF technology requirements for user equipment. In Proceedings of the 2008 IEEE Compound Semiconductor Integrated Circuits Symposium, Monterey, CA, USA, 12–15 October 2008; pp. 1–4.
11. Claus, M.; Gross, D.; Haferlach, M.; Schröter, M. Critical review of CNTFET compact models. *TechConnect Briefs* **2012**, *2*, 770–775.
12. Schroter, M.; Claus, M.; Sakalas, P.; Haferlach, M.; Wang, D. Carbon nanotube FET technology for radio-frequency electronics: State-of-the-art overview. *IEEE J. Electron Devices Soc.* **2013**, *1*, 9–20. [CrossRef]
13. Raychowdhury, A.; Mukhopadhyay, S.; Roy, K. A circuit-compatible model of ballistic carbon nanotube field-effect transistors. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2004**, *23*, 1411–1420. [CrossRef]
14. Deng, J.; Wong, H.S.P. A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: Model of the intrinsic channel region. *IEEE Trans. Electron Devices* **2007**, *54*, 3186–3194. [CrossRef]
15. Deng, J.; Wong, H.S.P. A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part II: Full device model and circuit performance benchmarking. *IEEE Trans. Electron Devices* **2007**, *54*, 3195–3205. [CrossRef]
16. Frégonèse, S.; d'Honincthun, H.C.; Goguet, J.; Maneux, C.; Zimmer, T.; Bourgoin, J.P.; Dollfus, P.; Galdin-Retailleau, S. Computationally efficient physics-based compact CNTFET model for circuit design. *IEEE Trans. Electron Devices* **2008**, *55*, 1317–1327. [CrossRef]
17. Frégonèse, S.; Maneux, C.; Zimmer, T. Implementation of tunneling phenomena in a CNTFET compact model. *IEEE Trans. Electron Devices* **2009**, *56*, 2224–2231. [CrossRef]
18. Frégonèse, S.; Maneux, C.; Zimmer, T. A compact model for dual-gate one-dimensional FET: Application to carbon-nanotube FETs. *IEEE Trans. Electron Devices* **2010**, *58*, 206–215. [CrossRef]
19. Gelao, G.; Marani, R.; Diana, R.; Perri, A.G. A semiempirical SPICE model for n-type conventional CNTFETs. *IEEE Trans. Nanotechnol.* **2010**, *10*, 506–512. [CrossRef]
20. Luo, J.; Wei, L.; Lee, C.S.; Franklin, A.D.; Guan, X.; Pop, E.; Antoniadis, D.A.; Wong, H.S.P. Compact model for carbon nanotube field-effect transistors including nonidealities and calibrated with experimental data down to 9-nm gate length. *IEEE Trans. Electron Devices* **2013**, *60*, 1834–1843. [CrossRef]
21. Yamacli, S.; Avci, M. Accurate SPICE compatible CNT interconnect and CNTFET models for circuit design and simulation. *Math. Comput. Model.* **2013**, *58*, 368–378. [CrossRef]
22. Saberkari, A.; Shirmohammadli, V.; Yagoub, M.C. A 3–6 GHz current reused noise canceling low noise amplifier for WLAN and WPAN applications. *Wirel. Pers. Commun.* **2016**, *86*, 1359–1376. [CrossRef]
23. Kim, J.; Hoyos, S.; Silva-Martinez, J. Wideband common-gate CMOS LNA employing dual negative feedback with simultaneous noise, gain, and bandwidth optimization. *IEEE Trans. Microw. Theory Tech.* **2010**, *58*, 2340–2351. [CrossRef]
24. Eron, M.; Lin, S.; Wang, D.; Schroter, M.; Kempf, P. L-band carbon nanotube transistor amplifier. *Electron. Lett.* **2011**, *47*, 265–266. [CrossRef]
25. Saberkari, A.; Khorgami, O.; Bagheri, J.; Madec, M.; Hosseini-Golgoo, S.M.; Alarcón-Cot, E. Design of broadband CNFET LNA based on extracted I–V closed-form equation. *IEEE Trans. Nanotechnol.* **2018**, *17*, 731–742. [CrossRef]

26. Yu, H.; Chen, Y.; Boon, C.C.; Mak, P.I.; Martins, R.P. A 0.096-mm^2 1–20-GHz triple-path noise-canceling common-gate common-source LNA with dual complementary pMOS–nMOS configuration. *IEEE Trans. Microw. Theory Tech.* **2020**, *68*, 144–159. [CrossRef]
27. Deng, H.; Feng, H.; Zhang, N. A 0.03–3GHz inductorless wideband low noise amplifier in 65nm CMOS. In Proceedings of the 2020 IEEE 3rd International Conference on Electronics Technology (ICET), Chengdu, China, 8–12 May 2020; pp. 79–82.
28. Gao, H.; Shi, J.; Lin, F. A wideband LNA with Gm-boosted and noise cancel technique. In Proceedings of the 2020 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA), Nanjing, China, 23–25 November 2020; pp. 17–18.
29. Belmas, F.; Hameau, F.; Fournier, J.M. A 1.3 mW 20 dB gain low power inductorless LNA with 4 dB noise figure for 2.45 GHz ISM band. In Proceedings of the 2011 IEEE Radio Frequency Integrated Circuits Symposium, Baltimore, MD, USA, 5–7 June 2011; pp. 1–4.
30. Tu, Y.; Wang, C. A 4–6 GHz current-mode differential transconductance wide band LNA. In Proceedings of the 2011 International Conference on Electrical and Control Engineering, Yichang, China, 16–18 September 2011; pp. 2821–2824.
31. Duong, Q.T.; Dąbrowski, J.J. Low noise transconductance amplifier design for continuous-time ΣΔ wideband frontend. In Proceedings of the 2011 20th European Conference on Circuit Theory and Design (ECCTD), Linkoping, Sweden, 29–31 August 2011; pp. 825–828.
32. Chen, J.S.; Lu, C.W.; Yin, P.Y.; Hsia, C.; Liu, J.Y.C. A wideband transconductance enhancement CMOS LNA with multiple feedback technique. In Proceedings of the 2015 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS), Tel-Aviv, Israel, 2–4 November 2015; pp. 1–4.
33. Cordova, D.; Bampi, S.; Fabris, E. A CMOS low noise transconductance amplifier for 1–6 GHz bands. *Analog Integr. Circuits Signal Process.* **2016**, *89*, 585–592. [CrossRef]
34. Arshad, S.; Ramzan, R.; ul Wahab, Q. Wideband common gate LNA with novel input matching technique. In Proceedings of the 2016 5th International Conference on Modern Circuits and Systems Technologies (MOCAST), Thessaloniki, Greece, 12–14 May 2016; pp. 1–4.
35. Duong, Q.T.; Alvandpour, A. Low noise linear and wideband transconductance amplifier design for current-mode frontend. In Proceedings of the 2014 International Symposium on Integrated Circuits (ISIC), Singapore, 10–12 December 2014; pp. 476–479.
36. Luo, L.; Li, Z.; Cheng, G.; He, X.; He, B. A 0.2–2.5 GHz resistive feedback LNA with current reuse transconductance boosting technique in 0.18-µm CMOS. In Proceedings of the 2017 IEEE 15th Student Conference on Research and Development (SCOReD), Kuala Lumpur, Malaysia, 13–14 December 2017; pp. 424–427.
37. Falaschetti, L.; Mencarelli, D.; Pelagalli, N.; Crippa, P.; Biagetti, G.; Turchetti, C.; Deligeorgis, G.; Pierantoni, L. A compact and robust technique for the modeling and parameter extraction of carbon nanotube field effect transistors. *Electronics* **2020**, *9*, 2199. [CrossRef]
38. Landauer, G.M.; González, J.L. Radio-frequency performance of carbon nanotube-based devices and circuits considering noise and process variation. *IEEE Trans. Nanotechnol.* **2014**, *13*, 228–237. [CrossRef]