Università Politecnica delle Marche
Scuola di Dottorato di Ricerca in Scienze dell'Ingegneria
Curriculum in Ingegneria Biomedica, Elettronica e delle Telecomunicazioni

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Technologies for the Integration of Waveguide Components and Antennas on Printed Circuit Boards

Ph.D. Dissertation of:

Francesco Bigelli

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to my Father, Giorgio

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Abstract

In this research work I present the feasibility study on the realization of a class of devices in SIW (Substrate Integrated Waveguide) technology for ICT application at microwave frequencies. With this technology it is possible to obtain, by the traditional processes for the printed circuits manufacturing, integrated components with quality factors greater than the microstrip and the stripline.
SIW technology is very promising because it permits to obtain compact, low cost and self-shielding guiding structures and hence, guides components. Although many papers, presented in literature, strengthen these qualities, this technology did not lead to an industrial production today, even at low volumes.

This work is part of the formation project annexed to its research project, entitled "Integrated Waveguide (SIW) technologies development for microwave ICT applications" in collaboration with the Politecnico of Bari, Università Politecnica delle Marche and SOMACIS SpA, a worldwide PCB (Printed Circuit Board) industry with forty years of experience in the highly technological sector of high-mix and low-volume.

As this hopeful technology allows a drastic reduction in size and costs, qualities that are well suited to the increasing market needs, the project aims to design and realize a class of product ranging from filter, hybrids, "frequency-shaping" components and antenna. SIW technology could also permit to produce in a large scale expensive and complicated products like the automotive and defense radars. Moreover, in the market of civil telecommunication, it could be possible to replace the standard and bulky TV dishes with planar array of antenna that are more competitive and could have a wide spread. Such array could also be fully integrated in the roof like it happens for the solar panels, this advantage could drive people to opt for these new concept of satellite antennas. Indeed, it seems to be realistic to foresee a market of thousands of components overlooking the proper motivation to the success of the project.

The SIW technology permits to reproduce in a planar form, through rows of metallic holes, a traditional waveguide. Obviously, in these structures, the electromagnetic field travels into the dielectric and not in air. It is clear that this involves a sensible increase of the losses. Even if the dielectric losses are the dominant part, these are still enhanced from a high density of current localized in the metallic holes that constitute the lateral sidewalls.

In recent years several Substrate Integrated Waveguide devices such as antennas [1-2], filters, and couplers [3-4, 5-6] have been reported in literature. SIW technology is a good technique for designing and fabricating microwave and millimeter-wave devices and circuits [7-21]. However, an industrial use of SIW components still requires an essential phase of systematic study.
Therefore the first objective of this study consists in optimization of technologies most suitable for the realization of this components.

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Fig. 5.19: Top-diagonal view of the Hybrid antenna. In detail the transition between the feed line and radiators

Chapter 1.

Introduction

1.1. Substrate Integrated Waveguide (SIW) technology

In high frequency applications, the microstrip, that is the most popular technology on the printed circuits, is not efficient when the wavelength becomes small; therefore, the manufacturing of such devices requires tolerances on the production process more and more limited.

Vice versa, at high frequencies (above the GHz), the waveguides are preferred, thanks to their low losses and to the high power handling. Conversely, waveguides suffer of an elevated manufacturing cost, their realization processing is complicated and their weight and size are not negligible (Fig. 1.1a).
The problem of the dimensions can be reduced inserting a bar of dielectric material that fully or partially fills the guide, inside the waveguide wherever possible. (Fig. 1.1b). In this way the guided wavelength gets smaller, if compared to the case in the vacuum, in relation to $\sqrt{\boldsymbol{\varepsilon_r}}$ or rather then the relative dielectric constant of the material.
By the way, the insertion of dielectric material, implies many consequences, beyond the others, like the arise of losses due to the non-idealities of the filling material and a reduced power handling, but elevated in any case. Once again, the reduction of power handling is due to the dielectric material, that could also damage itself if the electric field inside the guide exceeds its dielectric strength, since an electric arc is generated. Due to the heat and the pressure incited by the ionization of molecules inside the material, the dielectric may also suffer of permanent alterations.

Meeting market demands, then, require devices with high quality factor and small clutters, the Substrate Integrated Waveguide arisen (Fig. 1.1c). It deals of a transition between the microstrip and the Dielectric Filled Waveguide (DFW), practically the DFW is converted in a SIW through the use of metallic holes placed along the lateral walls of the guide realizing an electrical connection with the ground planes surrounding the dielectric, so it is possible to confine the electromagnetic field inside of it.

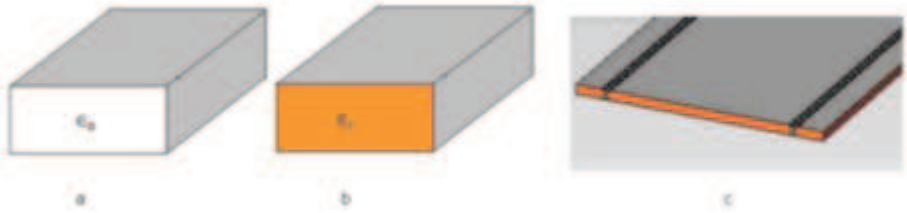

Fig.1.1: a) Traditional hollow Rectangular Waveguide (RWG)
b) Dielectric Filled Waveguide (DFW)
c) Substrate Integrated Waveguide (SIW)

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As the metallic holes, named vias, that constitute the lateral sidewall, discontinuous by nature, the Transverse Magnetic (TM) modes cannot be supported on this structure; similarly, the same consideration is made for the Transverse Electric modes TE_{nm} with $n \neq 0$. Therefore, the dominant mode of a Substrate Integrated Waveguide is the TE_{10}.
Although the SIW looks like a complex structure, it can be considered in every way a DFW, wherever is possible to find a binding between the widths of the above-mentioned structures, which have the same cutoff frequency. For a rectangular waveguide filled with a material of relative permittivity ε_r, the cutoff frequency of an arbitrary mode with indexes m and n is given by the relation (1.1)

$$\mathbf{f_{cmn}} = \frac{\mathbf{c}}{\mathbf{2\pi\sqrt{\varepsilon_r}}} \sqrt{\left(\frac{\mathbf{m\,\pi}}{\mathbf{a}}\right)^2 + \left(\frac{\mathbf{n\,\pi}}{\mathbf{b}}\right)^2} \qquad (1.1)$$

Where a and b are the dimensions of the broad and narrow wall respectively.

The paper of Cassivi et. al, "Dispersion characteristics of substrate integrated rectangular waveguide" [22], shows an empirical law that puts in relation the width of a SIW and the width of a DFW with the same propagation characteristics. This relation is:

$$\mathbf{a_s} = \mathbf{a_d} + \frac{\mathbf{d^2}}{\mathbf{0.95\,p}} \qquad (1.2)$$

here, a_s is the width of a SIW waveguide (considered the centers of vias in the opposite rows), while a_d is the width of a DFW with the same cutoff frequency (Fig. 1.2), d the via's diameter and p their pitch (Fig. 1.3).
Another relation was proposed in [23]

$$\mathbf{a_s} = \frac{\mathbf{2\,a_d}}{\boldsymbol{\pi}} \mathbf{cot^{-1}} \left(\frac{\boldsymbol{\pi p}}{\mathbf{4\,a_d}} \mathbf{ln} \frac{\mathbf{p}}{\mathbf{2d}}\right) \qquad (1.3)$$

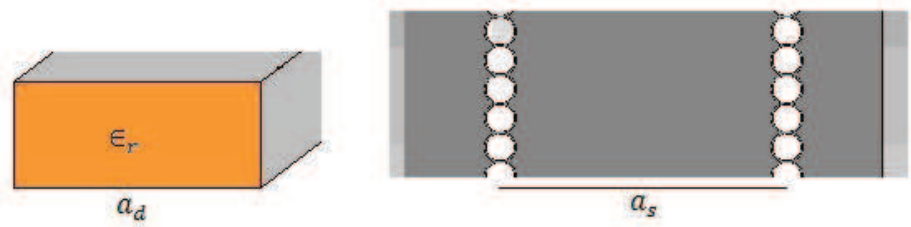


Fig. 1.2: Equivalence between a SIW and a DFW

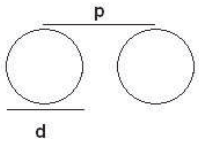


Fig. 1.3: Geometry of the vias, here are evidenced the diameter (d) and the pitch (p)

Naturally, the pitch of the vias and their diameter are two essential parameters of the SIW waveguide and shall comply some binding in order to consider a SIW like a DFW, that is easier to design. In the same paper [22] cited previously, the two conditions that permit to satisfy this equivalence are:

$$\mathbf{d} < \frac{\lambda_g}{5} \qquad (1.4)$$

$$\mathbf{p} < \mathbf{2d} \qquad (1.5)$$

Where λ_g is the wavelength at the working frequency of the DFW filled with a material with a relative permittivity of ε_r, that is:

$$\boldsymbol{\lambda_g} = \frac{2\pi}{\sqrt{\frac{\varepsilon_r (2\pi f)^2}{c^2} - \left(\frac{\pi}{a_d}\right)^2}} \qquad (1.6)$$

Here c is the speed of light.

Evidently, SIW propagative characteristics cannot be fully understood without consider the effects of the dissipated power into the dielectric and through the consecutive vias. Moreover, a limited part of the electromagnetic energy is irradiated across the vias. These aspects are fundamental because give rise to a reduction of the quality factor, reducing the advantages of the SIWs.

The loss mechanism in SIW technology is determined by 3 main factors:

1) Losses in the conductor, due to the finite conductivity of the copper;
2) Losses in the dielectric;
3) Radiation Losses, due to a slow leakage through the vias.

The behavior of the SIW conductor losses is absolutely equivalent to what happens in the traditional metallic waveguides and it is due to the induced currents from the electric field established inside the guide. Since then, is not possible to act on the conductibility of the material once the conductor is chosen, the only solution to reduce this factor is to increase the thickness of the guide. In this way the electric field will be weaker and subsequently, as well as its induced currents. The variation of other parameters in the geometry of SIWs exhibits a negligible effect in the metal losses.
Differently, dielectric losses, are not related to the guide geometry, but depend uniquely on the dissipation factor (D_f) that is an electrical property of the material. The macroscopic effect of the dielectric dissipation, is an effect of the microscopic structure of the material.
Finally, the radiation losses can be minimized if the pitch of consecutive vias is fairly tight, a good confinement is get if the pitch is inferior to the double of the via's diameter and, so, the latter it is minimized if is strictly equal.

Chapter 2.

Material characterization

Chapter 1 described the SIW technology and its state of art. Naturally, the realization of components with this methodology cannot disregard the practical on the construction process and all the non-idealities that brings with it. One of the most serious problem, however, lies in the uncertainty of the value of dielectric constants of substrates provided by the manufacturers. Designing SIW components must take into account of these dispersions and must therefore rely on specific topologies that allow making a robust design.

Base materials used in the production of Printed Circuit Boards (PCB) possess many thermal, physical, mechanical and electrical properties. Some of the most important for the classification of base materials will be introduced in this chapter.
Most of these properties are determined through tests, which follow standard procedures regulated by the IPC – Association Connecting Electronic Industries (IPC-TM-650).

2.1. Physical characteristics of materials for Printed Circuits

2.1.1. Glass transition temperature

The glass transition temperature, usually indicated by the symbol T_g, represents the value of temperature below, which an amorphous material behaves like a "glassy" solid. In practice, the glass transition temperature marks the border between the amorphous and vitreous state and the amorphous deformable state that is liquid and characterized from a high viscosity. The glass transition is not a thermodynamic transition, but a kinetic one, at which does not coincide any change in the disposition of atoms and molecules, as it happens during the transition phase from solid-crystalline to liquid. While glassy substances or inorganic minerals, such as the silica, possess a specific value of T_g, the thermoplastic polymers may have an additional T_g, below which become rigid and brittle, assuming an easy tendency to shatter. Also, at temperatures higher than T_g, such polymers possess elasticity and ability to undergo plastic deformation without encountering fractures, a characteristic which is exploited in the technology. The values of glass transition, which are commonly referred, are actually average values, depending on the gradient with which the cooling is performed and also on the distribution of the average molecular weights. In addition, the presence of additives may also influence the T_g of the system.

The T_g of a resin system has two main implications, including the thermal expansion and a measure of the degree of cure of the resin system.

2.1.1.1. Thermal expansion

All the materials change their physical dimension as the temperature changes. The rate at which the material considered expanded is lower below the glass transition temperature than above. The thermo-mechanical analysis (TMA) is used to measure the dimensional variations of a material. TMA is a procedure to measure the dimensional changes versus the temperature. Typically, the behaviour of a resin-based material, or a system is shown in Figure 2.1.

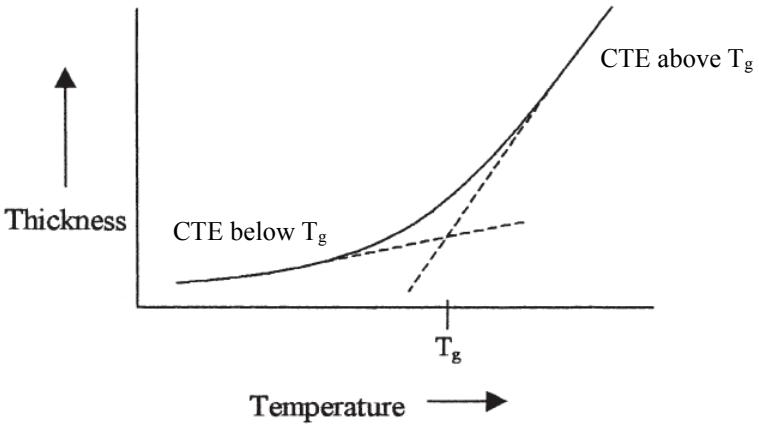


Fig. 2.1: Expansion of a resin-based material vs. temperature

The physical properties of laminates can begin to change as T_g is approached, this is because some of the molecular bonds are effected. From the diagram 2.1, it is very clear that the slopes of the curve below and above the T_g, have two very different behaviours. Once the T_g is reached, and if the resin is completely cured, the material conserves the properties of rigidity and cannot come back to the softened state. In the datasheet of the materials, the values of thermal expansion in the plane of the laminate (CTE_{xy}) and in quote (CTE_z) are distinguished. CTE values, but in particular the CTE_z, are sensible parameters of the circuit because they can affect the reliability of the finished circuit. Low values of CTE_z are desirable, since less thermal expansion will stress the plated holes that run through the z axis of the printed circuit. Many thermal cycles over the time can also cause circuit failures due to the separation of the conductor from the hole wall, or in the worst of cases to crack the conductor up to generate an open.
While it is certain that higher values of T_g involve a high expansion only at high temperatures, the total expansion of the circuit can vary from material to material. Not the only T_g has to be considered during the planning of the material to be used, or rather the total expansion of the system that is a function of T_g and CTE.

Moreover, it is well known that high-T_g materials are more brittle respect low-T_g materials and this has some implications, first of all during the drilling. High-T_g materials are drilled with a lower angular speed respect the low-T_g materials. Some CTE value of typical materials are listed in the Table 2.1.

Material	T_g (°C)	z-Axis expansion (% from 50 to 260°C)	CTE_{xy} (ppm/°C from -40 to 125°C)
FR-4 epoxy	140	4.5	12-16
Filled FR-4 epoxy	155	3.7	12-14
High-Tg FR-4 epoxy	180	3.7	10-14
BT/epoxy blend	185	3.75	10-14
Low-D_k epoxy blend	210	3.5	10-14
Cyanate ester	250	2.7	11-13
Polyimide	250	1.75	12-15

Tab. 2.1: Thermal expansion values of some common base material

The benchmark methodology for the CTE measurements is the IPC-TM-650, method 2.4.24C. When determining the coefficient of thermal expansion of a laminate, the temperature scan must scan at a temperature sufficiently lower than the specified temperature range, which the CTE is being determined to allow the heat rate to stabilize.

2.1.1.2. Degree of cure

Many base materials contain reactive site on their molecular structure that reacts with the heat. The heating of the resin system causes the reactive sites to cross-link or bond together. The curing of the resin system changes brings physical changes in the material, proportionally to the occur of the cross-linking, including increasing in the temperature of glass transition. Once most of the reactive sites have cross-linked, the material is finally fully cured and its properties are stable over the time and versus the temperature.
The TMA is not the unique test method to measure the T_g and the degree of cure of a material. There are two other thermal analysis techniques: differential scanning calorimetry (DSC) and the dynamic mechanical analysis (DMA).

DSC measures heat flow absorption or emission from a sample versus the temperature. The heat absorbed changes as the temperature increases across the T_g of the resin. DSC can be used to establish the degree of cure achieved by a resin system. The test procedure is specified in IPC-TM-650, method 2.4.25C.
DMA measures the modulus of the material on varying of the temperature. With this test method an oscillatory stress on the sample is applied while the temperature is increased during the test. The capacity of the material to store mechanical strain energy changes during the increase of temperature, this property determines the T_g of the resin system. The test procedure is specified in IPC-TM-650, method 2.4.24.2.

Non-fully cured materials can cause reliability problems on the finished circuit. One of the most popular effect is the excess of resin smear during the drilling process inside the hole being formed. As it will be shown in the chapter 3, a good cleaning of the holes is fundamental to avoid undesired metallisation voids that can generate in some cases the loss of electrical continuity of the plated hole. Another aspect that could affect the consistency of a non-properly cured circuit is an increase of the z-axis thermal expansion. Even in this case the plated holes are over stressed and may also cause malfunctions of the final product.
From T_g measurements it is also possible to determine the degree of cure of a resin system. This assumption is based on the fact that increased cross-linking requires greater amounts of heat to weaken the bonds in the molecular structure. A method to verify the cure of the resin system foresees two thermal analyses, such as TMA but on the same sample. The degree of cure of the system is measured by comparing the two different T_g of each experiment. The first thermal cycle is to promote any additional cross linking in the resin, the second thermal cycle is to verify that all the cross linking is performed and the material reached a stable molecular disposition. If the degree of cure is complete, the difference between the two T_g will be limited to some degree Celsius. Even negative values of "delta T_g", defined as difference between the Tg at the second measure less the Tg at the first measure, indicate a good polymerization of the material. Conversely if delta T_g is positive, it means that the system is not fully cured and, again, this could also affect the functionalities of the boards.

2.2. Dielectric constant measurements

One of the most important properties of a laminate is its capability to store electric charge. When a material is subjected to an electric files, causing the polarization of the molecules, electric dipole moments are established and the electric flux (**D**) is augmented. The dielectric constant, also known as permittivity of a material, is then responsible of the origin of a polarization vector (**P**) inside the material.

$$D = \varepsilon_0 E + P = \varepsilon_0(1 + \chi)E = \varepsilon E \qquad (2.1)$$

$$\varepsilon = \varepsilon' - j\varepsilon'' \qquad (2.2)$$

χ is the electric susceptibility and is a complex quantity. ε', the real part of the permittivity is called D_k, instead its imaginary part is called dissipation factor or D_f. The imaginary part corresponds to a phase shift of **P** relative to **E** and leads to the attenuation of the signal passing through the medium. The dielectric constant is commonly referred to the real part of the permittivity, this can generate some ambiguity. In the datasheet the only terminologies used are D_k and D_f. The value of D_k, is a number that is derived indirectly from a test method and may vary according to the different situations. Moreover, D_k and D_f are not pure constants, but depend on many factors, beyond the others temperature, humidity, homogeneity and above all the frequency. Besides, in many cases, especially at microwave frequencies, the vectors **P** and **E** are not orientated in the same direction, in this case the medium is said anisotropic and it becomes difficult to measure the anisotropy matrix.

At the moment there is not a single technique that can accurately characterize all materials over all the dependencies above mentioned. It is possible to distinguish two main families of techniques, depending on the band in which the measures are performed.
Narrow band techniques, are based on resonant measurement and the permittivity is determined from measurements of the resonance frequency and the quality factor, where the quality factor for a resonant cavity is defined as $Q = f_0/\Delta f$, with f_0 the resonant frequency and Δf is the frequency difference between 3dB points, as shown in Figure 2.2.

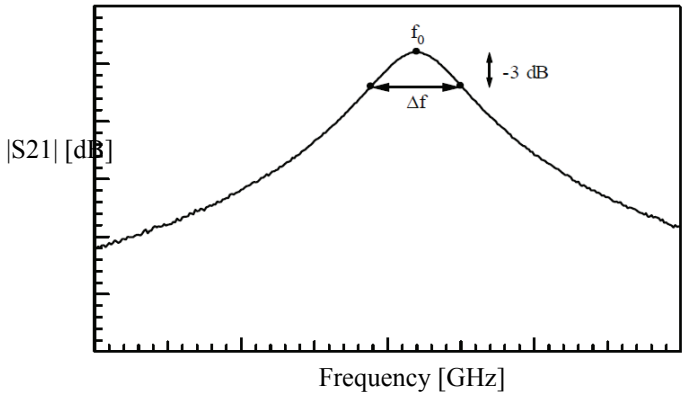


Fig. 2.2: Measuring resonant frequency and Q

With such methods, it is possible to obtain very accurate values (with an error of 0.2 – 0.5%) of D_k and D_f but limited only to a unique portion of the spectrum.
Another family of tests, based on transmission line measurements, permit to obtain values of D_k and D_f over a spread spectrum of frequencies, but with less accuracy, which is around 1 – 10%.
An exact knowledge of the dielectric constant is fundamental to have a good expectation that the actual circuit performance will mirror the modelled performance.

2.2.1. Narrow band measurement methods

2.2.1.1. IPC TM-650 2.5.5.5c

The test method IPC TM-650 2.5.5.5c, better known as clamped stripline resonator in X band, is one of the most commonly used test method on the testing of raw laminate. This test consists in the construction of a strip line resonator and basing on the quality factor measured, D_k and D_f are derived.
The specimen is prepared by staking:

- The top copper foil;
- A copper clad laminate fully etched in one side and with the resonator imaged in the other side (Figure 2.3), the dimension of the resonator depends on the nominal value of dielectric constant to be verified, according to Table 2.2.
- A copper clad laminate fully etched in both sides;
- The bottom copper foil.

The specimen is then clamped at a determinate force (4.45 kN) to reduce the entrapped air in the clamped fixture that involves an under estimation of the value D_k.

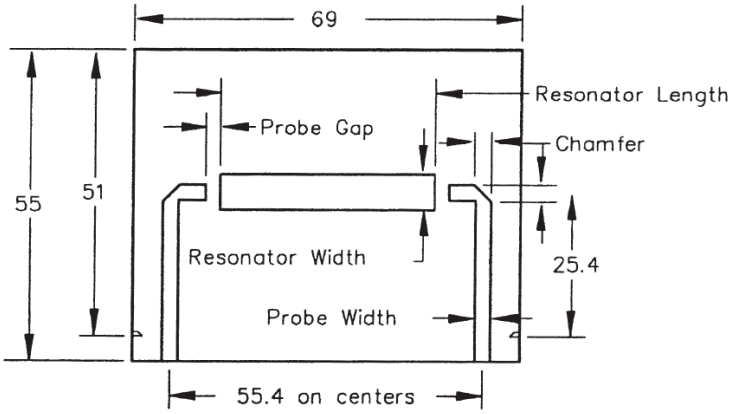


Fig. 2.3: Generalized resonator pattern card matching the nominal permittivity of material to be tested, all the quotes in millimeters

Nom.ε_r	Nom. Thk.	Pattern Card Thk.	Probe Width	Chambfer X, Y	Probe Gap	Resonator Width	Resonator length 4 node	1/Qc Conductor loss
2.20	1.59	0.22	2.74	3.05	2.54	6.35	38.1	0.00055
2.33	1.59	0.22	2.67	2.92	2.54	6.35	38.1	0.00055
2.50	1.59	0.22	2.49	2.79	2.54	6.35	38.1	0.00055
3.0	1.59	0.22	2.13	2.41	2.54	5.08	31.8	0.00058
3.5	1.59	0.22	1.85	2.16	2.54	5.08	31.8	0.00058
4.0	1.59	0.22	1.62	1.93	2.54	5.08	31.8	0.00058
4.5	1.59	0.22	1.45	1.73	2.54	5.08	31.8	0.00058
6.0	1.59	0.22	1.07	1.30	2.29	3.81	25.4	0.00062
6.0	1.27	0.22	0.86	1.07	2.29	3.81	25.4	0.00072
10.5	1.27	0.22	0.81	0.54	2.03	2.54	17.3	0.00079

Tab. 2.2: Dimensions for stripline test pattern in millimeters

The two probes of the specimen are connected through SMA connector to a network analyser, with which are determined: the resonant frequency of the resonator (maximum transmission) f_0 and the two frequencies f_1, f_2, related to the point at -3dB below the maximum located at f_0.
At the resonance, the electrical length of the resonator is a multiple of half wavelength and the dielectric constant can be easily determined as follow:

$$\varepsilon_r = \left[n\, c / \left(2 f_0 (L + \Delta L)\right)\right]^2 \qquad (2.3)$$

Where: n is the number of half wavelength along the strip;
c is the speed of light;
L is the length of the resonator;
ΔL is a correction factor that account the fringing field at the ends of the resonator.

The normative 2.5.5.5c furnishes three different methods to estimate ΔL that must be experimentally determined.

The loss tangent is obtained with the formula:

$$\tan\delta = \frac{1}{Q} - \frac{1}{Q_c} = \frac{f_2 - f_1}{f_0} - \frac{1}{Q_c} \qquad (2.4)$$

1/Q is the total loss due to the dielectric, copper and copper-dielectric interface, while $1/Q_c$ is the loss relative to the copper only and it is tabulated in Table 2.2.

This test determines the value of D_k in the direction perpendicular to the plane of the laminate.

2.2.1.2. Split cylinder resonator

The split cylinder resonator method is another narrow band method, using a cylindrical cavity partially loaded with an unclad dielectric laminate. In such cylindrical cavity it is excited the mode TE_{011} through two small coupling loops placed in each halves. The thickness and the dielectric constant of material inside the cavity will influence the resonant frequency. To derive the permittivity, it is measured the resonant frequency of the cavity with no material inside, a second measurement is done but in this case the etched laminate is inserted in the middle of the cavity, between the two halves, the setup of the test is shown in Figure 2.4.

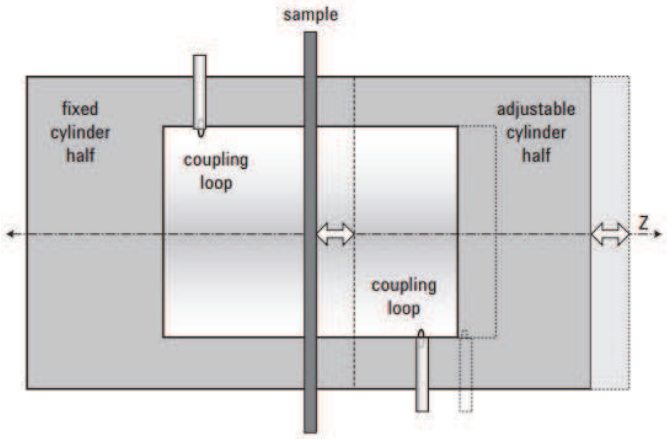


Fig. 2.4: Split cylinder resonator – experimental setup

So, when the sample is placed in the cavity, the resonant frequency of the whole system will be shifted towards low frequencies, respect the case without the sample. This shift can be attributable uniquely to the real part of the dielectric constant, D_k uniquely. The imaginary part, D_f, will be calculated in the same way of the method described in 2.2.1.1.

Some common base material such as standard FR4, high-Tg FR4 and ceramic materials were measured at the frequency of around 10 GHz with the Agilent 85072A split cylinder resonator at the Politecnico di Bari. The measures were then compared to the values declared from the supplier, results are listed in the table below (Table 2.3).

		From datasheet			Measured with the split cylinder resonator method		
Material	Thickness [mm]	Frequency [GHz]	D_k	D_f	Frequency [GHz]	D_k	D_f
MCL BE 67 G	1.076	10	4.4	0.01	9.132	4.45	0.0040
FR 408 HR	1.440	10	3.65	0.009	9.074	3.74	0.0029
IT 158	1.075	10	4	0.018	9.139	4.43	0.0039
IT 180	1.000	10	4.1	0.016	9.231	4.34	0.0048
ROGER 4350	1.490	10	3.48	0.004	9.088	3.57	0.0019

Tab. 2.3: Split cylinder resonator Dk measurements vs. datasheet values

Even if the resonant frequency measured is around 9 GHz, it is possible to compare the measures with the values declared in the datasheet.

With this method it is possible to notice a very good correlation between theoretical data and measured data. The deviations of D_k and D_f from theoretical data can be attributable to the fringing fields in the sample region outside of the cylindrical waveguide section that was ignored to keep the method much simple as possible. It exists also an improved theoretical model, based on the mode-matching method that takes into account this factor.

2.2.1.3. SIW resonator

Another resonant method for the achievement of the permittivity of a material, foresees the realization of a resonator in SIW technology. This test method is particularly representative because the measure is performed on a structure similar to the device that will be designed.
Such that resonator was designed to have a resonant frequency within the Digital Video Broadcasting – Satellite (DVB – S), where frequencies of interest are located. The resonator is 9 mm long and the guide is 10.25 mm wide. At the end of the guide, two transitions were designed to match the SMA connector to the guide in all the entire band considered, the designed rules for these transitions will be shown in the chapter 4.
The CAD model and the prototype realized are shown in Figure. 2.5.

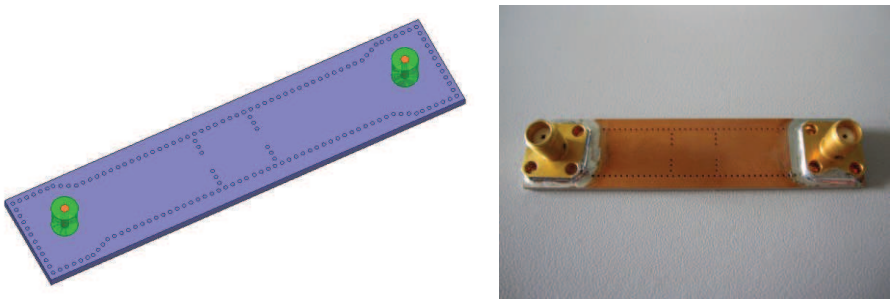


Fig. 2.5: SIW resonator – CAD model on the left and the prototype on the right

The laminate used in this experiment is the Taconic RF-35A2, a teflon-based material with low losses. The resonator thus realized, was measured and its frequency response compared with the relative simulations.

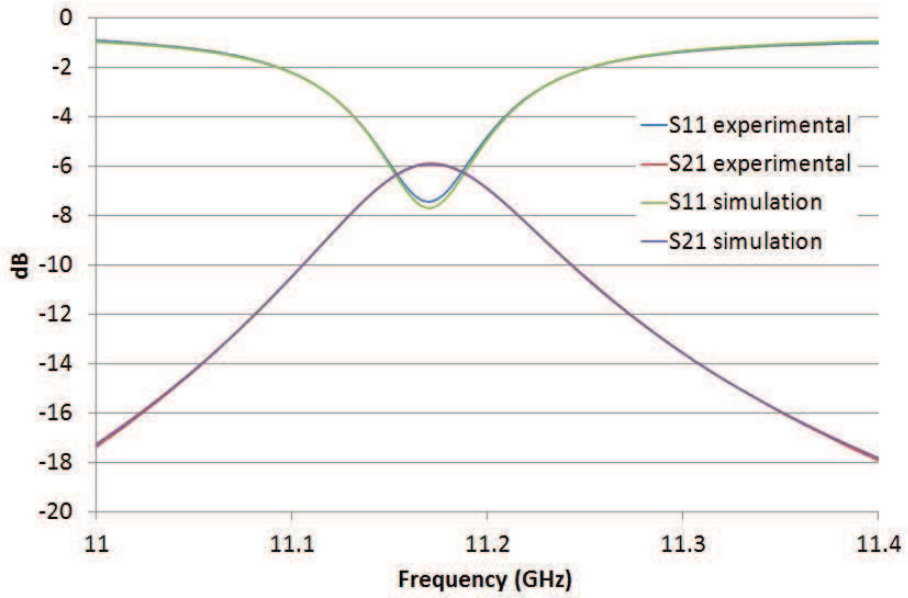


Fig. 2.6: SIW resonator frequency response – experimental vs. simulated results

The resonant frequency lies at 11.1745 GHz, where the signal is attenuated of 5.93 dB. The bandwidth measured considering the frequencies at -3 dB respect the resonant frequency is 110MHz. With this data it is possible to calculate the quality factor "loaded" (Q_L) and "unloaded" (Q_U) of the cavity as follow:

$$Q_L = \frac{1}{FBW} = \frac{f_0}{\Delta f} = 101 \qquad (2.5)$$

$$Q_U = \frac{Q_L}{1-|S_{21}|} = 202 \qquad (2.6)$$

At this stage, to obtain the dielectric constant, the same structure was simulated through the Finite Element Method (FEM) based software, Ansys HFSS, where the two parameters D_k and D_f were varied, starting from their nominal values (D_k = 3.5, D_f = 0.0015), up to get the most superimposable frequency response to the experimental data. Such condition is obtained for Dk = 3.48 and Df = 0.0038, with these values the superposition is excellent.

Though the real part of the dielectric constant is very close to that declared from the supplier, the imaginary part measured shows a non-negligible deviation, which could affect negatively the devices designed with the material. This difference could be attributable to three different factors:

1) Different test methods for calculation of dielectric constant. The supplier used the IPC-650 2.5.5.5.1, a modified version of 2.5.5.5, instead of the SIW resonator method;
2) The test method used from the supplier is performed at 10 GHz, instead with this method the measurements are made around 11 GHz and it is well known that losses rise as the frequency rise;
3) As the Taconic RF-35A2 is a teflon-based laminate, it is hygroscopic, this means that tends to store humidity inside. The molecules of water entrapped in the material cause a sensible augment of losses and then a higher D_f.
4) Effects due to a non-perfect welding of the connectors.

2.2.2. Broadband measurement methods

2.2.2.1. Partially loaded waveguide

The first broad band method for the extraction of the dielectric constant is based on a transmission-line model. The specimen is prepared starting from an unclad dielectric material with dimensions as to fit, in the most accurate manner, the interior of a waveguide. For measurements in the X-band, a WR90 rectangular waveguide was used, and samples of different material were resized at a dimensions of a = 22.86 mm and b = 10.16 mm, the thickness of the materials was measured. The samples are introduced inside the waveguide, and the latter is connected to a network analyser.
Under a circuital point of view, the structure (Figure 2.7) is represented from the series of three-line section, of which, two of them in air and the central filled with the dielectric.

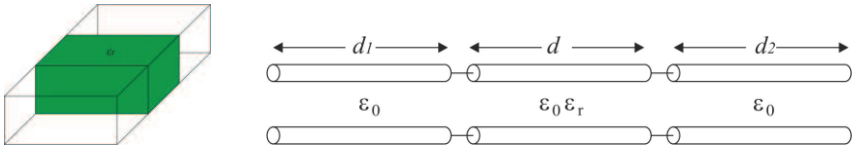


Fig. 2.7: Schematic representation of the measurement setup on the left and circuital representation on the right

Measurements were taken with a network analyser at Dipartimento di Ingegneria dell'Informazione of Università Politecnica delle Marche, the calibration of the instruments were performed in WR90.
Since the two line sections in the air have the same cross section of the guide calibrate, they introduce only a phase shift. Obviously, such assumption can be made if two line sections in the air are fairly short and do not introduce losses comparable with the section filled with the dielectric.
So, the problem is reduced to a simple segment of line filled with a dielectric of thickness d, that is represented by the transmission matrix ABCD:

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} \cos(\beta\, d) & j\, z_0 \sin(\beta\, d) \\ \frac{j\, z_0 \sin(\beta\, d)}{z_0} & \cos(\beta\, d) \end{pmatrix} \qquad (2.7)$$

Where z_0 is the characteristic impedance normalized respect the source impedance, that is 50 Ω, β is the complex propagation constant of the section filled with dielectric.
The non-normalized impedance Z_0 for the mode TE_{10} in the central section is:

$$Z_0 = \frac{\omega\, \mu_0}{\beta} \qquad (2.8)$$

In the two hollow sections, it is considered the constant β_0.

$$Z_0^0 = \frac{\omega\, \mu_0}{\beta_0} \qquad (2.9)$$

From the correspondence between the matrix ABCD and the matrix S, with the conversion formulas it is possible to derive the theoretic parameters S_{11} and S_{21}.

$$S_{11} = \frac{\frac{\beta}{\beta_0} - \frac{\beta_0}{\beta}}{\frac{2}{\tan(\beta\, d)} + \frac{\beta}{\beta_0} - \frac{\beta_0}{\beta}} \qquad (2.10)$$

$$S_{21} = \frac{2}{\left(\frac{2}{\tan(\beta\, d)} + \frac{\beta}{\beta_0} - \frac{\beta_0}{\beta}\right)\sin(\beta\, d)} \qquad (2.11)$$

Considering also that the hollow line segments and the S-parameter of the two ports:

$$S'_{11} = S_{11}\, e^{-2j\beta_0 d_1} \qquad (2.12)$$

$$S'_{22} = S_{22}\, e^{-2j\beta_0 d_2} \qquad (2.13)$$

$$S'_{21} = S'_{12} = S_{21}\, e^{-j\beta_0 (d_1 + d_2)} \qquad (2.14)$$

Where $d_1 + d_2 = d_{tot} - d$, the parameter S'_{21} does not depend on the position, but only on the sample thickness and the length of guide containing it. Solving the equation (2.12) or (2.13) or (2.14) respect β substituting instead of the S-parameter, the experimental data and using the formula (2.15) it is easily obtainable the dielectric constant, that is:

$$\varepsilon_r = \frac{\left(\frac{\pi}{a}\right)^2 + \beta^2}{K_0^2} = \varepsilon' - j\, \varepsilon'' = \varepsilon(1 - \tan(\delta)) \qquad (2.15)$$

The same material measures with the split cylinder resonator were measured and the data are collected in Table 2.4.

		From datasheet			Measured with the transmission line method		
Material	Thickness [mm]	Frequency [GHz]	D_k	D_f	Frequency [GHz]	D_k	D_f
MCL BE 67 G	1.076	10	4.4	0.01	8.5 – 12.5	4.78	0.01
FR 408 HR	1.440	10	3.65	0.009	8.5 – 12.5	4.05	0.01
IT 158	1.075	10	4	0.018	8.5 – 12.5	4.79	0.015
IT 180	1.000	10	4.1	0.016	8.5 – 12.5	4.55	0.02
ROGER 4350	1.490	10	3.48	0.004	8.5 – 12.5	3.77	0.005

Tab. 2.4: Transmission line Dk measurements vs. datasheet values

Another significant material (the reasons will be clear in the paragraph 2.5), experimentally validated with this method is the Taconic RF-35A2, already measured with the SIW resonator. Three sample of such material were prepared as shown in the Figure 2.8:

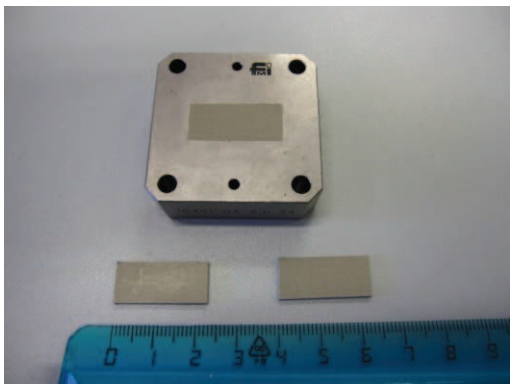


Fig. 2.8: Specimens of RF-35A2 and the waveguide WR90

All the samples have a thickness of 1.52, with a deviation of 8μm. Each sample was experimentally characterized and an average of the three measures is shown in Figure. 2.9.

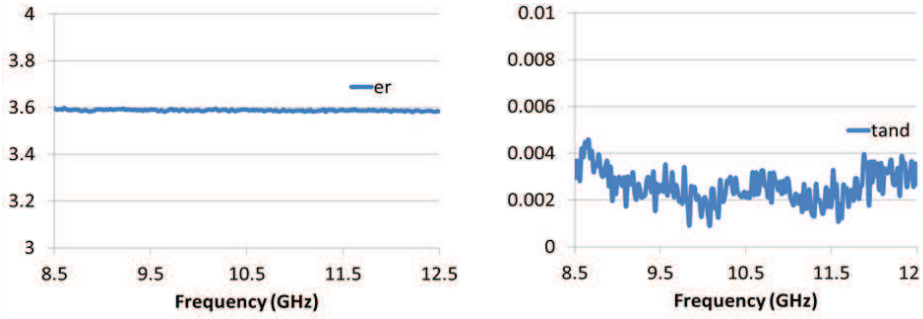


Fig. 2.9: Average of three samples of Taconic RF35-A2, D_k on the left and D_f on the right

From the measurements it is noticeable that the value D_k, here around 3.59, is slightly greater that the value declared from the supplier that is 3.5 as well as the dissipation factor D_f, 0.0025 measured versus 0.0015 from the datasheet.

2.2.2.2. Differential phase length

The second broad band test method used to achieve the permittivity of the material under study is called "differential phase length method". This test exploits the difference of phases between two transmission lines with different physical length. In literature [24], this method is widely treated with the microstrips, but it can be extended also to other electrical transmission lines where their closed form solution is well known. In this work two Substrate Integrated Waveguide segment of lines (Figure 2.10) of different lengths, 109.234 mm and 59.234 mm respectively were realized on a substrate of Taconic RF-35A2 with nominal relative permittivity of 3.5.

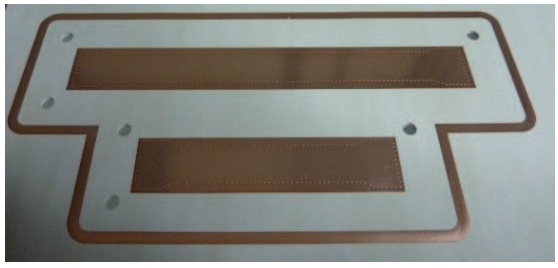


Fig. 2.10: Two segments of line in SIW technology with different lengths

For each line, the relationship between the physical length and the electrical phase length is given by:

$$\Phi_1 = 2\pi f \frac{\sqrt{\varepsilon_{eff}}}{c} L_1 \qquad (2.16)$$

$$\Phi_2 = 2\pi f \frac{\sqrt{\varepsilon_{eff}}}{c} L_2 \qquad (2.17)$$

Where c is the speed of light, f the frequency and Φ_1,Φ_2, L_1, L_2 are the phase and physical lengths of the two lines. ε_{eff} is common to the two waveguides because it is realized on the same medium and with the same technology.
To remove the electrical length of the fixture, and also undesired effects of the connectors feeding the lines, the equation (2.17) is subtracted from (2.16), with $\Delta\Phi = \Phi_1 - \Phi_2$ and $\Delta L = L_1 - L_2$.

$$\Delta\Phi = 2\pi f \frac{\sqrt{\varepsilon_{eff}}}{c} \Delta L \qquad (2.18)$$

Such equation emphasizes that once the frequency and the medium are fixed, the dependency of the difference of phase length of the two waveguide is affected uniquely from their difference of physical length.

The latter equation can be rearranged to explicit the effective permittivity ε_{eff}.

$$\varepsilon_{eff} = \left[\frac{\Delta\Phi}{\Delta L}\frac{c}{2\pi f}\right]^2 \qquad (2.19)$$

For a SIW waveguide of physical width a_s, and then for a dielectric waveguide with equivalent width a_d, with the only fundamental mode in propagation, the two identities are valid:

$$k_c = \frac{\pi}{a_d} \qquad (2.20)$$

$$k_0 = \frac{2\pi f}{c} \qquad (2.21)$$

Where k_0 and k_c are the wavenumber and the cut-off wavenumber. From the effective permittivity, through the equations of the waveguides it can be easily derived the relative

permittivity of the filling material. A plot of the dielectric constant over the frequency is shown in Figure 2.11.

$$\varepsilon_r = D_k = \frac{{k_0}^2 \varepsilon_{eff} + {k_c}^2}{\left(\frac{2\pi f}{c}\right)^2} \qquad (2.22)$$

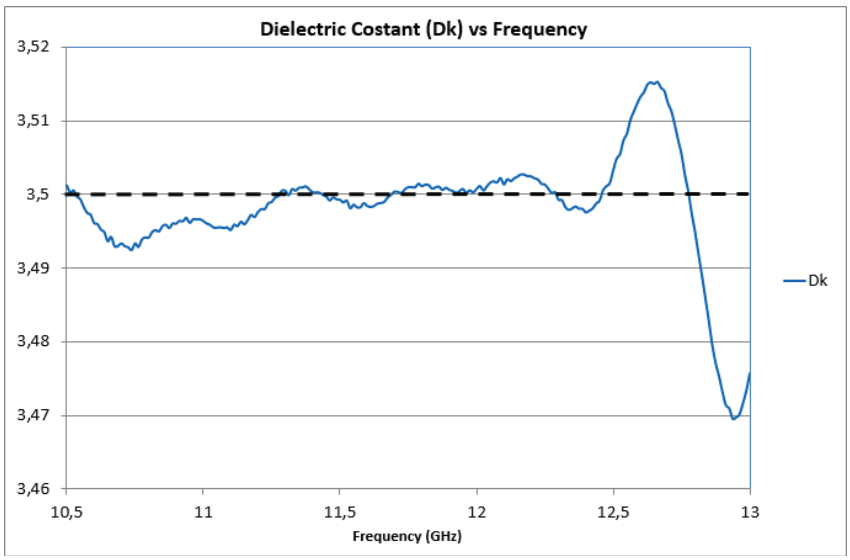


Fig. 2.11: Dielectric constant measured with the Differential Phase Length Method. The solid line is the permittivity calculated, the dashed line is the nominal value

2.3. Non-ideal effects of laminate structure

High Density Interconnection Printed Circuits Boards (HDI-PCB) are generally composed of a stack of many separate layers of laminates, properly processed, and interspersed with layers of prepreg that is a base material which does not already reach its glass transition temperature. Once that the entire stack is pressed, and the prepreg reaches the T_g, the resin presents inside the prepreg liquefies bonding together all the layers of the PCB. The structure thus obtained is solid and earns a certain mechanical strength.
Both the laminates and the prepregs are composed of various fiberglass cloths, bound together with epoxy resin. The number of combination of glass composition is wide (Figure 2.12), because many filament diameters, yarn types and density of textures are available. Generally speaking, the choice of a material rather than another is dictated on the thickness of the dielectric achievable with that texture (Table 2.5) and on the dielectric constant. Even if the glass and the resin have two very different dielectric constants (glass ≈ 6, resin ≈ 3.5), PCBs manufactures treat the laminate as a homogeneous electrical medium, with an average

permittivity taken from the material datasheet. Except for rare cases, the matter that the texture composed of perpendicular weaves and ordered fibers, realizing a periodically loaded dielectric medium, is completely ignored. High frequencies boards should take in consideration this inhomogeneity because they play an important role on their performances.

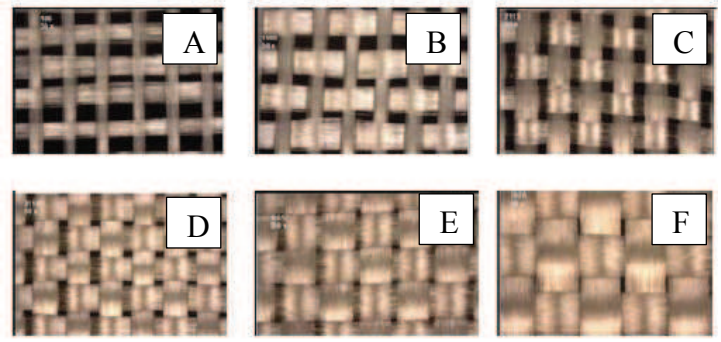


Fig. 2.12: Fiberglass cloth: a) 106, b) 1080, c) 2113, d) 2116, e) 1652, f) 7628

Glass style	Count warp	Count per Inch	Glass Thickness [µm]
106	56	56	38
1080	60	47	63
2113	60	56	73
2116	60	58	96
1652	52	52	114
7628	44	31	172

Tab. 2.5: Common fiberglass weave styles

2.3.1. Power loss due to periodic texture

A theoretical approach of the problem is described in [25]. Here a standard laminate was modelled as a medium composed of periodically varying dielectric properties. To simplify the model, an infinitely long one dimensional medium consisting of two alternating layers of material with different permittivity values was considered and a schematic representation is shown in Figure 2.13.

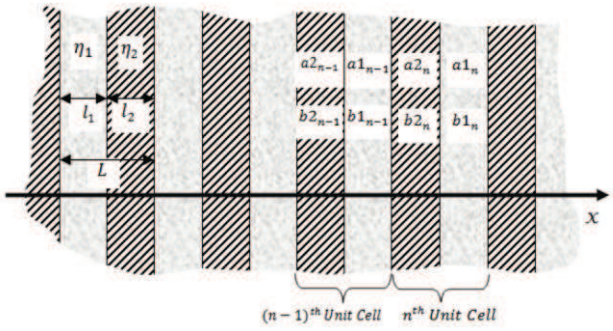


Fig. 2.13: Mono-dimensional representation of a laminate

Such laminate is composed of two different mediums, glass and resin for instance, with refraction indexes and lengths equal to η_1, l_1 and η_2, l_2 respectively. As the medium is periodic, it can be assumed that $\eta(x + L) = \eta(x)$. With this condition it is possible to apply the Floquet theorem to a component of field (2.23) propagating in the z direction, orthogonal to x.

$$E(x,z) = E(x)e^{j\beta z} \qquad (2.23)$$

Again, as the structure is periodic it can be applied the continuity of the fields at the interface of period L, that is:

$$E_k(x+L) = E_k(x) \qquad (2.24)$$

Applying the theorem, it can be written:

$$E_k(x,z) = E_k(x)e^{jKx}e^{j\beta z} \qquad (2.25)$$

$E_k(x,z)$ represents the electric field of a wave propagating in positive z direction, and depending on whether K is real or imaginary, the corresponding field will propagate or attenuate. K takes the name of "Block Wave Number" and depends on the frequency and on the period of the structure L. It can be derived [25] the Brillouin relation (2.26), from the name of one of the first researcher who studied the periodic wave propagation in atomic structures.

$$K(\beta,\omega) = \frac{1}{L}\cos^{-1}\left[\frac{1}{2}(A+D)\right] \qquad (2.26)$$

Where A and D are the diagonal element of the transmission matrix for TE mode propagation and their value is:

$$A = e^{-jk_1 l_1}\left[\cos(k_2 l_2) - \frac{1}{2}j\left(\frac{k_2}{k_1}+\frac{k_1}{k_2}\right)\sin(k_2 l_2)\right] \quad (2.27)$$

$$D = e^{jk_1 l_1}\left[\cos(k_2 l_2) + \frac{1}{2}j\left(\frac{k_2}{k_1}+\frac{k_1}{k_2}\right)\sin(k_2 l_2)\right] \quad (2.28)$$

With k_1 and k_2 the propagation constant in the two regions:

$$k_1 = \sqrt{\epsilon_{r1}\left(\frac{\omega}{c}\right)^2 - \beta^2} \qquad k_2 = \sqrt{\epsilon_{r2}\left(\frac{\omega}{c}\right)^2 - \beta^2} \qquad (2.29)$$

It can be concluded that for certain frequencies, namely for $\left|\frac{1}{2}(A+D)\right| > 1$, the block wave number K is imaginary and the wave is evanescent. In the same paper [25] a comparison between theoretical and simulated (with FEM method) Brillouin zones of an ideal composed medium (Figure. 2.14).

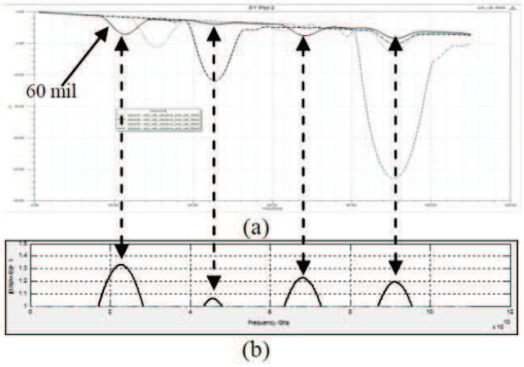


Fig. 2.14: Simulated and theoretical Brillouin zones. a) Insertion loss profiles of 60, 45, 30 and 15 mil period. b) theoretical evanescent zones of the 60 mil period. Courtesy of [25]

2.3.2. Signal integrity effects of fiber weave

The presence of block bands is due to the non-homogeneous nature of laminates. Another effect, neglected in most of cases even with boards at high data rate, is the "Fiber Weave Effect", better known as Intel effect.

In the paper "Fiber Weave Effect: Practical Impact Analysis and Mitigation Strategies" [26] the signal integrity effects due to the particular structure of laminates are investigated. Traces that runs overlapping the glass and the others overlapping the resin (Figure 2.15), will be subjected to different values of permittivity and thus will have different phase velocities ($v_p = c/\sqrt{\varepsilon_r}$): a signal routed over a glass bundle travels more slowly due to the higher ε_r.

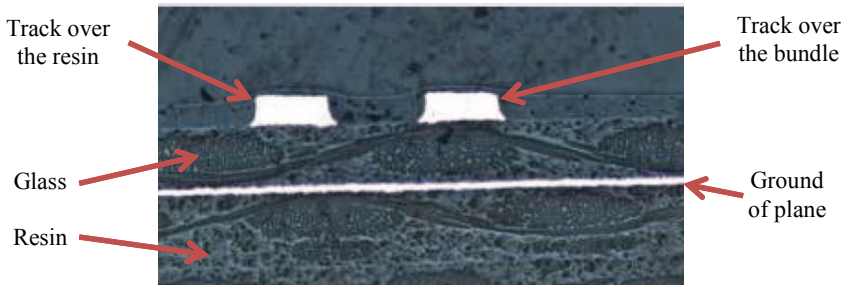


Fig. 2.15: Cross-section of two microstrips: one runs on the glass and the other one on the resin

The main effect of this track configuration is a degradation of the eye-diagram with a subsequent data-rate limitation. A practical approach consists of rotating the tracks of 10° respect the texture, in this way both traces will be subjected to a material with a non-well defined periodicity and will be exposed, on average, to the same material and then they will acquire the same phase velocity.

2.3.3. SIW texture dependency investigation

The majority of the composed materials for the PCB industry is inhomogeneous; this fact is attributable to the different permittivity of the bundles and the resin with which they are composed. More is the difference of the permittivity between the two composites and more pronounced are the effects due to the anisotropy, like the signal integrity and the presence of block bands but not only. The composite structure determines permittivity anisotropy, and the anisotropy for definition is the dependency on that property on the space that for a PCB is limited to the plane where the laminates lie inasmuch their thickness is negligible respect the length of the transmission lines arranged on the plane. Moreover, the dielectric constant does not depend only on the frequency but also on the measurement technique. In order to use a technique giving that it provides the most consistent results on the particular type of application, the Differential Phase method based on SIW guides, already addressed in 2.2.2.2. Because this kind of investigation is finalized to verify the value of the dielectric constant that will be used to design SIW prototypes, choosing a method based on SIW waveguides for sure will give the most faithful results.
Especially in high-speed interconnects there is a strong interest upon the performances of PCB realized on fiber-weave based materials, in this context the material Taconic RF-35A2 has been characterized. From the datasheet of this laminate it can be retrieved that it is composite of PTFE with an ultra-low content of fiberglass. Although, its geometric structure can be derived from cross and longitudinal microsections (Figure 2.16), by measuring the pitch and the z-distance of the bundle inside the PTFE matrix, it is not possible to achieve the exact value of permittivity of the two composites, and a simulation based on a simplified model of the laminate is not practicable. An experimental characterization of the material is then conducted.

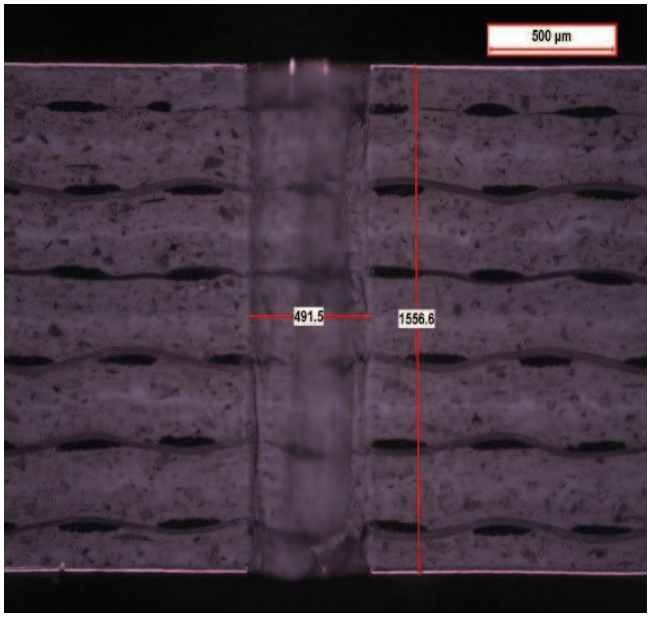


Fig. 2.16: Cross-section of a thought hole on a laminate of Taconic RF-35A2. It is noticeable the inhomogeneous structure of the material: in black the bundles and in purple the PTFE

The analysis for the verification of the anisotropy properties of the material is conducted through the composition on a panel of Taconic RF-35A2 of couples of line with different lengths (the same of Figure 2.10), but orientated with a different inclination respect the bundle. On the panel of Figure 2.17 there are 9 couples of lines tilted of 5°, 10°, 15°, 20°, 25°, 30°, 35°, 40°, and 45°. These angles are enough to characterize all the possible orientations of lines disposed on the plane with a pitch of 5° because the structure of the laminate is symmetrical respect the diagonal of the elementary cell of material, in fact an orientation of 50° is analogous of an orientation of 40°, 55° with 35° and so on.

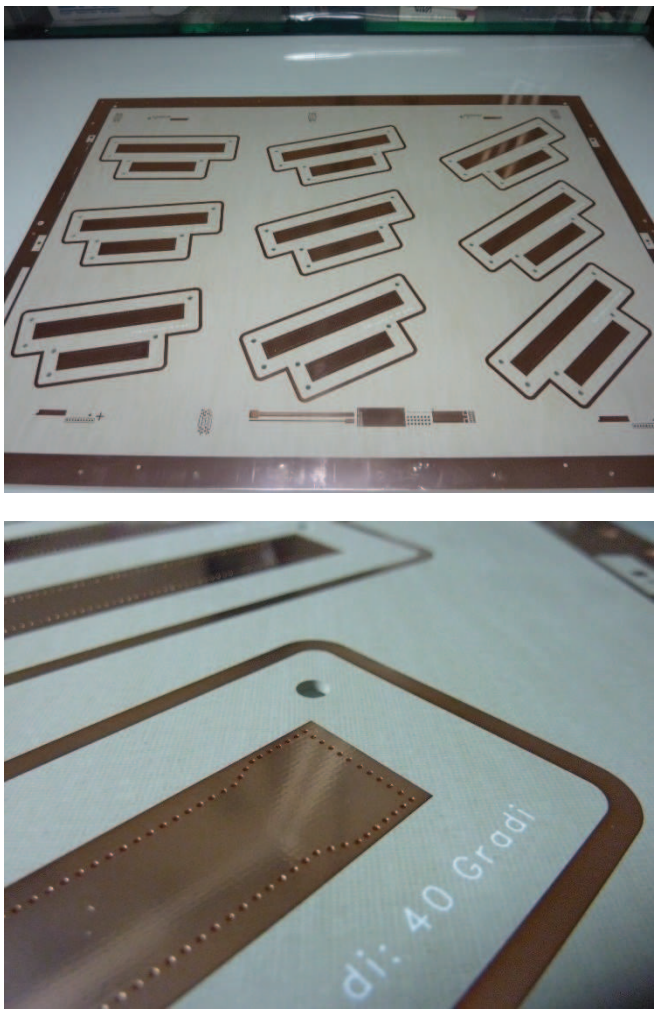


Fig. 2.17: Panel of Taconic RF-35A2 with couple of lines with different orientation respect the bundle. Below, a detail of line disposed with a tilt of 40°. Thanks to the bright material, the bundles externally (dark and parallel stripes) are visible

With the same methodology used in 2.2.2.2, the dielectric constant for each couple of lines has been derived. The graphs in Figure 2.18 show the trend of the permittivity versus the frequency and the variation of the permittivity at a fixed frequency for different orientations of the lines respect the bundle.

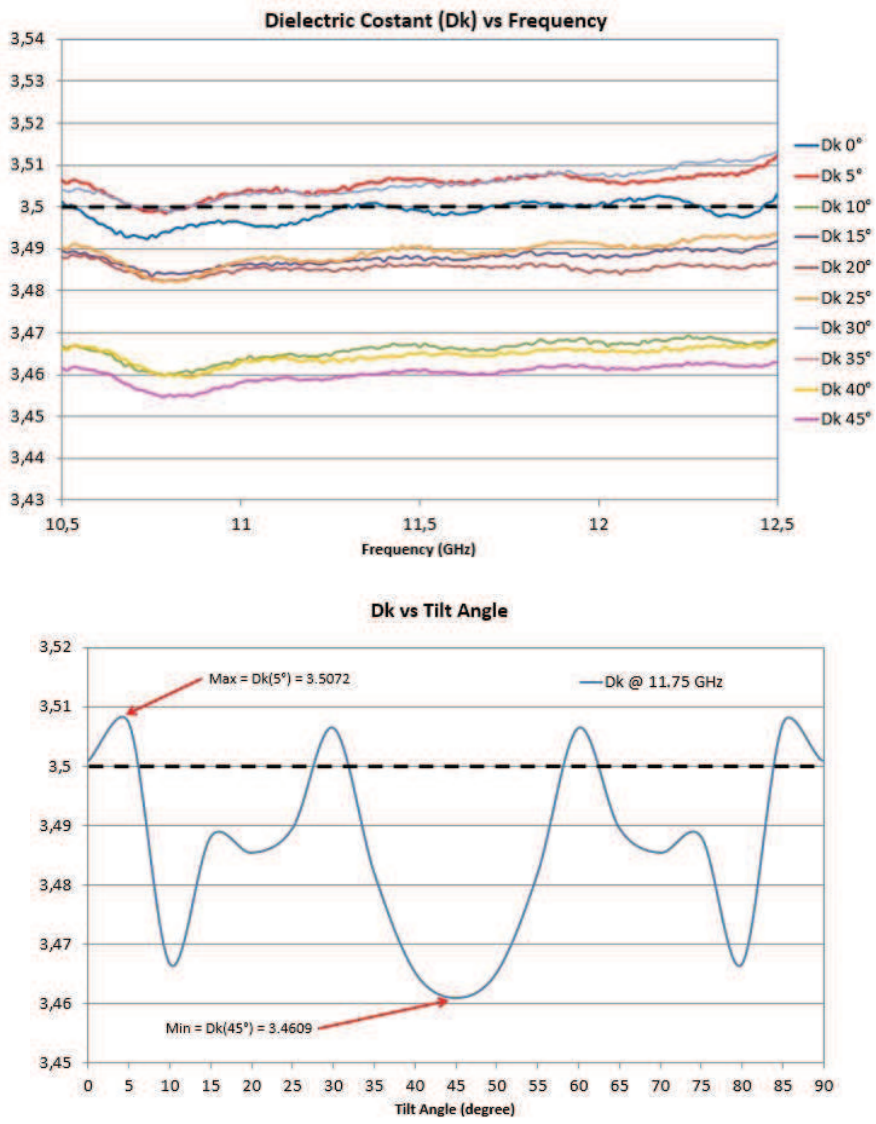


Fig. 2.18: Trend of the dielectric constant over frequency and over the tilt angle at the frequency of mid-band for the Taconic RF-35A2 in the DVB-S band. The black dashed lines represent the nominal value

From the charts in Figure 2.18 it can be observed that the permittivity value varies in a very limited range, the maximum deviation respect its nominal value is below the 1%. The material can be retained therefore isotropic with a very good approximation. Thanks to this assumption, in the simulation of the devices, the material can be defined as a constant and

not as a matrix, that is an important simplification under the aspects of computational complexity and then simulation times.

2.4. Material selection criteria

One fundamental aspect in this project concerns the selection of a material on which all the SIW devices realizing the antenna, beyond other filters, directional couplers and elementary radiators will be developed. Actually, it is not possible to define an "excellent" dielectric for every application, but it is possible to define a selection criterial customized of the type of antenna expected.
As it is well known, the SIWs are integrated waveguide made of two parallel rows of vias connecting two ground planes, the latter are interspersed with a substrate. In this way, the waveguides can be done in a traditional planar shape, compatibly with the existing technical processes. The SIWs exhibit propagation characteristics that are very similar to the traditional rectangular waveguide.

Since the SIW is attributable to DFW, three main project parameters are definable:

1) Dimensions;
2) Losses;
3) Cost.

The guides must be sized in such way to operate in the range 10.7 – 12.7 GHz, which is the band of the DVB-S. The intent is to achieve the condition of mono-modality of the guide, so it is necessary to impose the cutoff frequency of the TE_{10} below the minimum frequency of work, that is:

$$f_{c10} = \frac{1}{2a\sqrt{\mu\varepsilon}} = \frac{c_0}{2a\sqrt{\varepsilon_r}} \qquad (2.30)$$

Where:

- a is the width DFW considered;
- μ is the constant of magnetic permeability of the medium;
- ε is the absolute electric permittivity of the substrate;
- ε_r, or D_k is the relative dielectric constant;
- c_0 is the speed of light in the vacuum.

The effective width of the SIW equivalent to the DFW is obtainable through (1.2).

Since all the materials treated in this context are paramagnetic ($\mu_r = 1$), it has been possible to get the equality in the equation above (2.30). Reversing such formula respect ε_r, and setting an appropriate cutoff frequency to minimize the dispersion of the signal ($f_{min} > 1.3\ f_{c10}$, f_{min} is the lower frequency considered and fc_{10} is the cutoff frequency of the TE_{10}), it can be written:

$$a = \frac{c_0}{2f_{c10}a\sqrt{\varepsilon_r}} \quad (2.31)$$

This relation shows that the width of guide is inversely proportional to the square root of D_k. Take as an example an hollow waveguide with dimensions a = 22.86mm and b = 10.16mm (WR-90). This guide has a cutoff frequency of the first fundamental mode at about 6.5 GHz. The same waveguide filled with ITEQ IT-158 (standard FR4 with D_k = 4.6), with the same cutoff frequency, will be achieved with a dimension of the broad side of only 10.66 mm. the choice of material is crucial in maintaining compact the size of the devices: using a material with a high permittivity will be easier to optimize the arrangement of components on the substrate, and dually, realizing more compact devices, less material and then a lower cost per unit will be necessary. A second consequence of the choice of a material is that there are losses. In waveguides, there are two possible causes of loss: the dissipation in the conductors and in the dielectrics. In presence of real conductors, these, having a finite conductivity behave like resistors in series to the transmission line. These resistors dissipate part of the electromagnetic energy into heat, according to the Joule effect. The value of these resistors depends on the conductibility of the conductors and on the current induced on the latter, so, as it is not possible to intervene on the conductibility, unless using a different material ,the only choice is to use a sufficiently thick substrate. In this way the electric field inside the guide, will induce surface currents that are less intense than in the case of a thin laminate, it is then recommended, where possible, to use the maximum thickness available for a given dielectric. The second mechanism of loss, the dielectric losses, is related only to the type of material and the production process for the substrate manufacturing. The dielectric losses are taken into account by the use of the complex dielectric constant, where the imaginary part and the real part are linked together by the term tan(δ) or Df, a parameter normally given by the manufacturer of the substrate. In dielectric with losses, the propagation constant $\gamma = \alpha + j\beta$ has a non-null real part. This is equivalent to multiply the expressions relative to the ideal case (with no losses) for a multiplicative term $e^{-\alpha}$, such term, purely real and per unit length, attenuates the travelling wave inside the guide, thus reducing the signal level. Another consequence of a medium with losses is that the phase angle of the tensor of the characteristic impedance is not zero, in particular, it can assume value between 0 and 45 degrees.
Is such application it is recommended to select material with D_f as low as possible, in order to minimize the dielectric losses and maintaining dispersion limited especially in presence of broadband signals as in this case.

Typically, however, low loss material is soft (with a low permittivity), then the requirement of compactness and low losses are opposed to each other.
The third constraint is represented by the cost of the material. This parameter is critical to keep the price of the final product still contained.
Summarizing, a good material for this project purpose shall have:

1) High value of permittivity (D_k), to keep the dimension contained;
2) Low dissipation factor (D_f), to keep low the dielectric losses;
3) A low cost, to make the final product competitive.

Table 2.6 shows, three materials from a set of common material used in the PCB industry that are the "best in class" with respect to the characteristics considered.

Material	D_k	D_f	Price [Normalized to FR4]
Isola PCL 370 HR	**5.40**	0.035	2.27
Rogers Duroid 5880	2.20	**0.0009**	85.05
Iteq IT 158	4.60	0.016	**1**

Tab. 2.6: Three best in class materials

As on that, there is no material that encloses all these features, so it is necessary to find a compromise. For the choice of such this material, it has been defined a figure of merit (FoM) that takes into account the parameters above mentioned. Using the traditional method, it has defined a ratio in which the merit and demerit parameters numerator appear to the numerator and to the denominator respectively. For each material it was then attributed a score based on this criteria and the best material will be that with the highest value of FoM.

The material selection criteria is:

$$\mathrm{FoM} = \max\left\{\frac{\sqrt{D_k}}{cost\ e^{2K_0\sqrt{D_k D_f}}}\right\} \qquad (2.32)$$

In the numerator there is the square root of the relative dielectric constant, being inversely proportional to the width of the guides. In the denominator the price of the material and an exponential term proportional to the power loss in a DFW length 1m appear.
Of course, this value has no physical sense, but only serves to provide an indication for the choice of the material; it should not take as an absolute criterion.
In Table 2.7 all the materials considered, with the salient parameters and the FoM, are listed:

Material	Cost [Norm. FR4]	D_k	D_f	FoM
Rogers Duroid 5880	**85.65**	**2.20**	**0.0009**	**5.86E-12**
Taconic RF-35A2	**23.73**	**3.50**	**0.0015**	**2.98E-17**
Rogers 3202	122.40	3.02	0.0016	2.27E-17
Rogers 3035	128.57	3.50	0.0017	5.56E-19
Arlon TC350	30.96	3.50	0.0020	9.41E-20
Panasonic Megtron 6	23.54	3.61	0.0020	6.61E-20
Rogers 4003 C	31.59	3.38	0.0029	4.92E-23
Arlon FR 25 N	20.14	3.58	0.0035	1.14E-25
Rogers 4350 I	31.59	3.48	0.0037	4.16E-26
Panasonic Megtron 4	14.47	3.80	0.0050	6.18E-31
Hitachi MCL LX 67 Y	12.27	3.50	0.0061	1.21E-32
Nelco N4000 13 SI	7.27	3.70	0.0080	6.37E-38
Arlon 33 N	17.62	4.25	0.0090	2.76E-43
Hitachi MCL BE 76 G	2.86	4.40	0.0100	1.66E-45
Isola FR 408 HR	7.55	3.56	0.0130	4.07E-47
Iteq IT158	1.00	4.60	0.0160	3.38E-58
Iteq IT180	1.00	4.70	0.0180	2.68E-62
Panasonic R1566 W	2.08	5.40	0.0350	3.29E-93
Isola IS 420	2.27	5.40	0.0350	3.02R-93
Isola PCL 370 HR	2.27	5.40	0.0350	3.02E-93

Tab. 5.7: Whole set of the material considered

On the top of this list two particular materials, which have been chosen as candidates for the prototypes realization come to light. The Rogers Duroid 5880, despite its cost, has an exceptionally dissipation factor. The Taconic RF-35A2, has a dissipation factor less performant than the Duroid, but it permits to realize devices that are more compact and with a lower final cost.

Chapter 3.

PCB PTFE-based manufacturing process

The object of this chapter is the development of the most appropriate technology for the realization of SIW devices. The main problem is to achieve an optimal design, able to take into account the tolerances of machinery and properties of material used in production. They are, therefore, needed significant experimental investigations in order to refine the production process, leading the design of components.
Many different materials and processes can be used to manufacture SIW circuits. For very simple circuits, only a few processing steps are required. However, the degree of complexity does not depend on the layer count and on the dimension of track and space only, but also on the involved materials.
As a result, it is very hard to describe, except in the most general fashion, a common process usable for every circuit. In this chapter it is described first one of the basic process for the fabrication of PCBs, an analysis of the criticism that it takes with it, at the end a modified process with the proper correction actions.

3.1. Semi-additive process

By definition, a SIW circuit, is a double sided board with plated through-hole connecting the top and bottom layers. There are several methods and respective variations for creating copper circuits for SIW applications. One of the most used processes for the creation of double sided boards, but not only, is the semi-additive process.
As the name implies, this method is not fully additive (the addition is referred to the copper), it means that the copper is added selectively over the panel through an appropriate mask. The process normally involves the use of a laminate or a mass-lam (Figure 3.1a) that is perforated accordingly the drilling design (Figure 3.1b), then the panel is chemically activated (Figure 3.1c) and a thin layer of copper is deposited all over it (Figure 3.1d,e). The deposition of copper involves either the copper foil already present over the laminate and the bare dielectric surface of the holes. Subsequently a reverse mask of dry-film is applied (Figure 3.1f) and additional copper is plated onto the unmasked areas (Figure 3.1g), reaching the desired copper thickness. A thin layer of Tin, with function of etch-resist, is then applied over the copper and itwill protect it through the etching process. Then, the dry-film is stripped and the copper below it will be etched by an alkaline bath, leaving only the pattern that is protected from the etch-resist (Figure 3.1h). The last stage is the stripping of the Tin that will uncover the pattern grown. A detailed list of all the stages of the process is reported below.

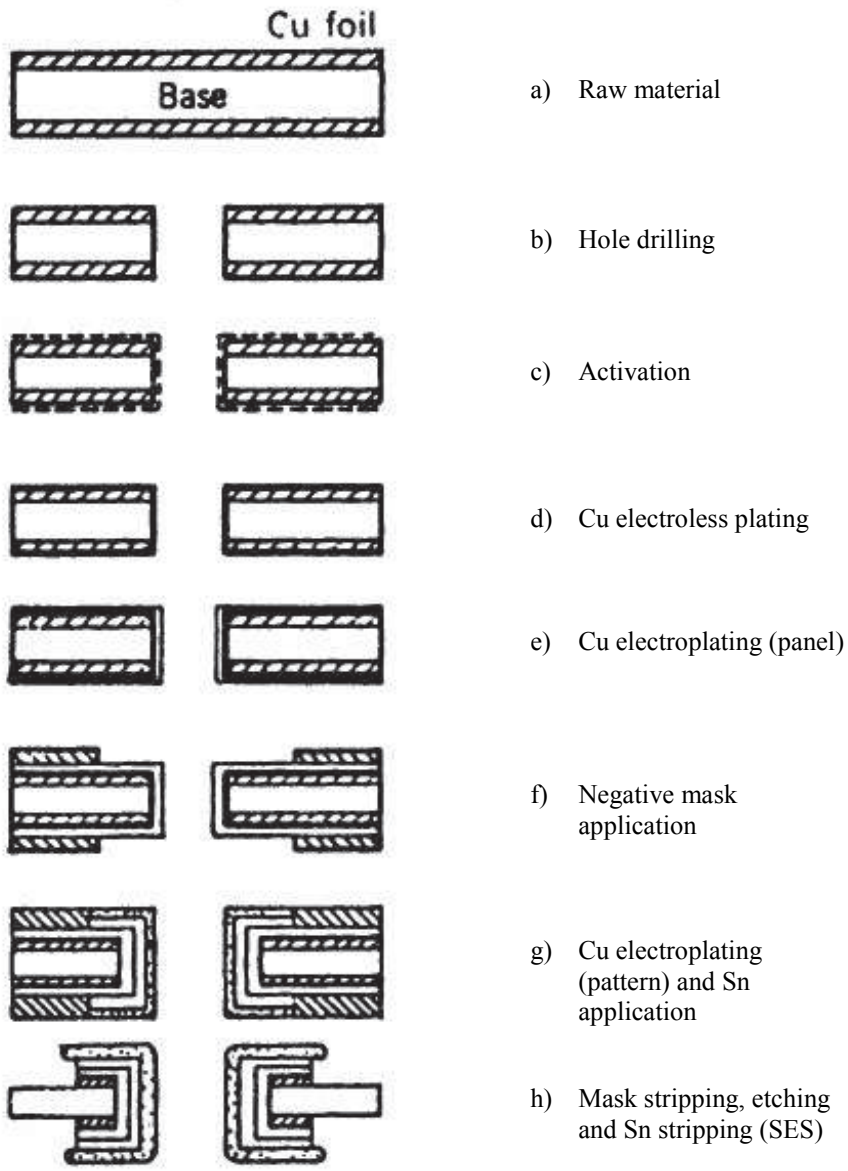


Fig. 3.1: Key manufacturing steps in pattern plating method. In detail the electroplating of a through hole with relative pads. Courtesy of [27]

The method pattern plating is very popular because the deposition of copper is localized only in the areas uncovered by the mask areas only, leaving, in the covered areas only few microns of copper (copper foil + electroless and panel electrolytic) to be etched. Such a method will be used for the formation of all the SIW circuits mentioned in this thesis.

3.1.1. Mechanical drilling

Drilling is a crucial stage of the fabrication process, since it allows the electrical connection between the various layers. In the present case, drilling allows the realization of rows of metallized holes parallel to the axis of the SIW for the guiding of fundamental mode.
The realization of all the prototypes has seen involved only the mechanical drilling on the base of the thickness of the laminate and drilling parameter such as the diameter and the pitch of the holes. In all manufactured devices, the diameters of the holes is in the range [500 - 1250] μm does not represent a critical parameter in itself, as opposed to the material used to realize them. The Taconic RF-35A2, which will be used for all the prototypes in this treatise, is a soft material and all the drilling imposed parameters shall be compatible to subsequent metalization process. The possible smearing residue in the holes is indicative of incorrect parameters in the setup of the machine. A non-optimal metalization due to wrong drilling parameters may compromise the signal confinement within the guide and then the devices themselves.

Most significant drilling parameters are:

- Diameter of the tip. In the normal process of realization of PTH (Plated Through Holes) the diameter of the tip must be increased by the estimation of the copper deposit inside the hole to obtain the finished bore diameter as requested by the customer. Conversely, in the case of SIWs, the diameter of the tip is chosen exactly equal to the diameter of the finished hole because the field is confined into the dielectric and the hole is not used for the assembly of components, but just as a barrier for the field.
- Angular speed. It is a parameter that depends on the tip diameter. It is not indicative the absolute value of angular speed, then, the value of peripheral speed of the blade and hence the penetration inside the material.
- Entry speed of the tip. It is a parameter that influences the uniformity of the hole. Excessive entry speeds of the tip may tear or deform the material before its drilling, contrary, a long persistent of the tip generates a lot of heat causing the fluidization of the resin inside the material. A non-uniform hole constitutes an uncertainty parameter in the success of the metalization. Generally soft materials require entry speeds higher than the rigid materials.
- Chip load. It is the amount of chip that each cutting surface of the blade is able to remove. It is related to the type of tip and to the angular speed.
- Entry material. Before the panel is drilled, it is packed between sheets of bakelite or aluminum. This arrangement has a dual function, that is to say facilitating the entry of the tip into the material and the removal of the chip during the spillage.
- Usury and cleaning of the tools. The status of the tools has to be kept under control to get an optimal drilling. Each tip has a maximum number of holes that can do,

beyond which the blade loses its effectiveness and may also cause the tearing of the material during the rotation. For soft materials, the cleanliness is also critical because the material tends to stick to the tip, making the chip removal more difficult. This reduces significantly the lifetime of the tips.

The preliminary drilling test over the Taconic RF-35A2 was performed on a laminate 1.52 mm thick and with holes by 500 µm of diameter. The quality of the holes was evaluated through an optical microscope, as shown in Figure 3.2.

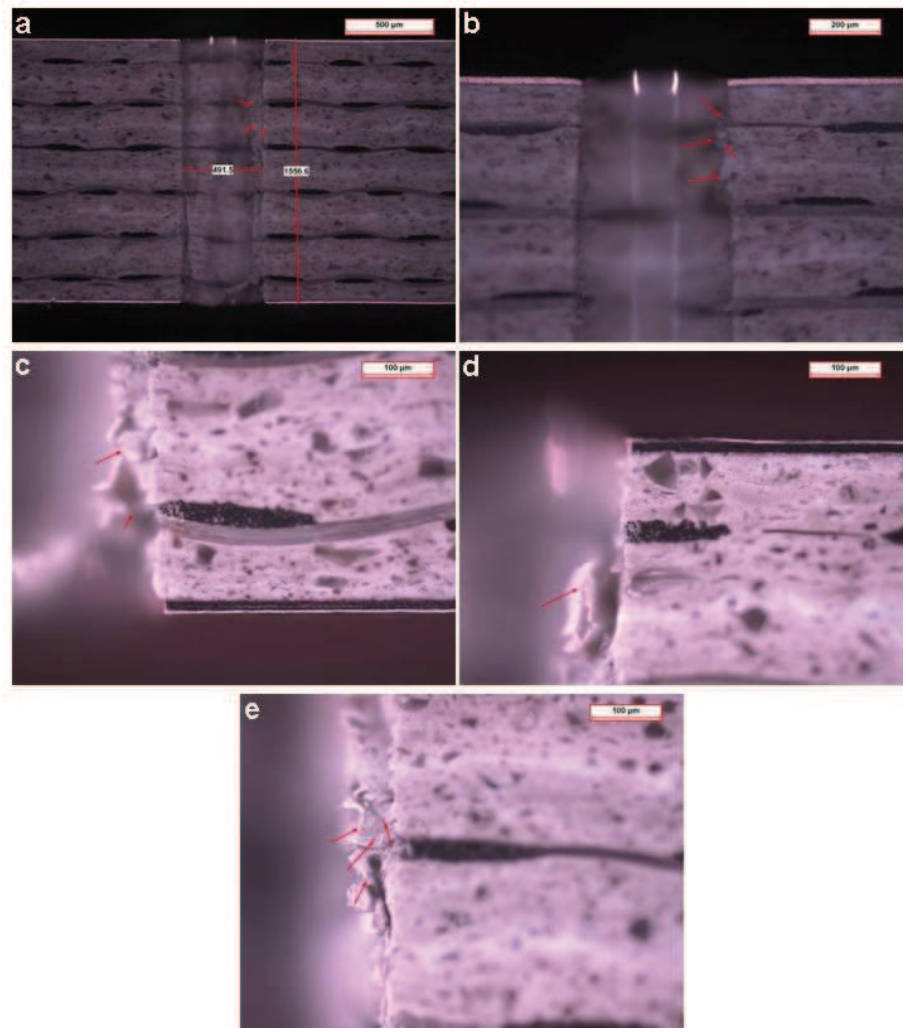


Fig. 3.2: Preliminary drilling test: a) microsection of the hole, b) c) d) e) details of residuals in its interior

It is quite clear that the cleaning of the hole is poor, in particular the residuals of materials, which have not been removed by the tip, are evident. By the way, it isn't widely known if the residuals will be removed by the chemical baths previous the metalization (activation – Figure 3.1c), and a metalization test is then attempted.
An easy, but very significant test to proof the goodness of a metalization of hole with a certain diameter is known as the "Daisy chain" scheme. Such a scheme foresees the drilling of 55000 through holes of appropriate diameter, neatly distributed on the laminate to be tested. The panel is composed of many cells, each of which is drilled with the smallest diameter (the most critical) of holes of the realized devices that is in this case 500 µm. Each cell constitutes a copper electrical path; in the specific case, it creates a serpentine path. In practice, the metalized holes allow the connection of the tracks between the upper side and the lower one, creating an electrical path on two levels (Figure 3.3).

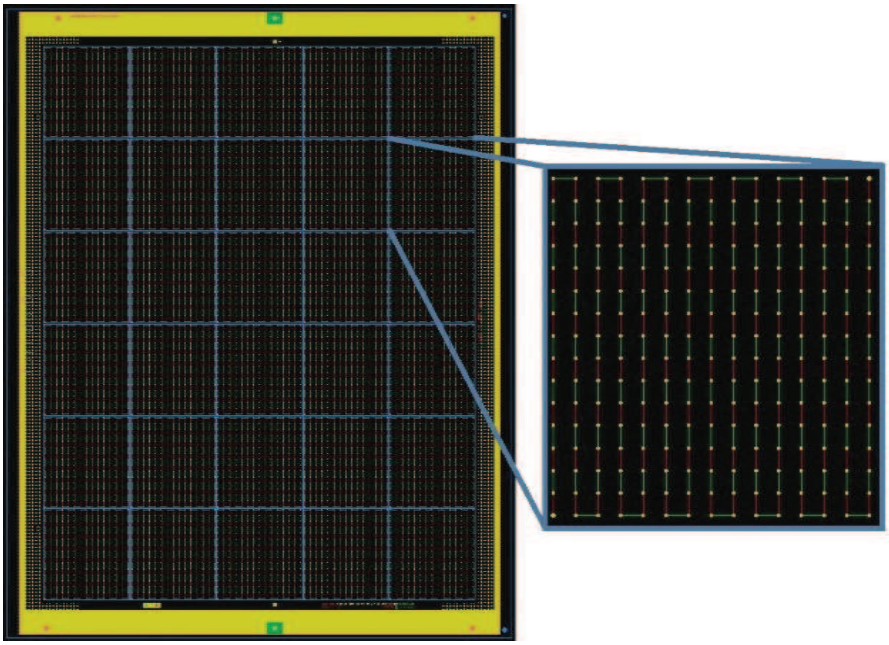


Fig. 3.3: The "Daisy chain" scheme. In detail the single cell formed of tracks on the top layer in red, tracks on the bottom layer in green and holes connecting all of them in yellow

To verify the quality of the metalization, each cell is tested by verifying the electrical continuity and by measuring the conductibility at the ends of the serpentine. In event of an electric open, a metallographic microsection should be performed in correspondence to investigate deeply the causes.
The problem of erroneous metalization, which is often believed to be due to problems encountered during the drilling stage, is also affected by a number of variables involved in the chemical process such as the cleaning process of holes with a chemical-physical attack.

A Daisy chain test is then performed on a laminate of Taconic RF-35A2 thick 1.52 mm, drilled and metallized with standard parameters (receipts are property of SOMACIS S.p.A.). From the first Daisy chain test emerged a huge number of electric opens and a microsection was gathered in their correspondence (Figure 3.4).

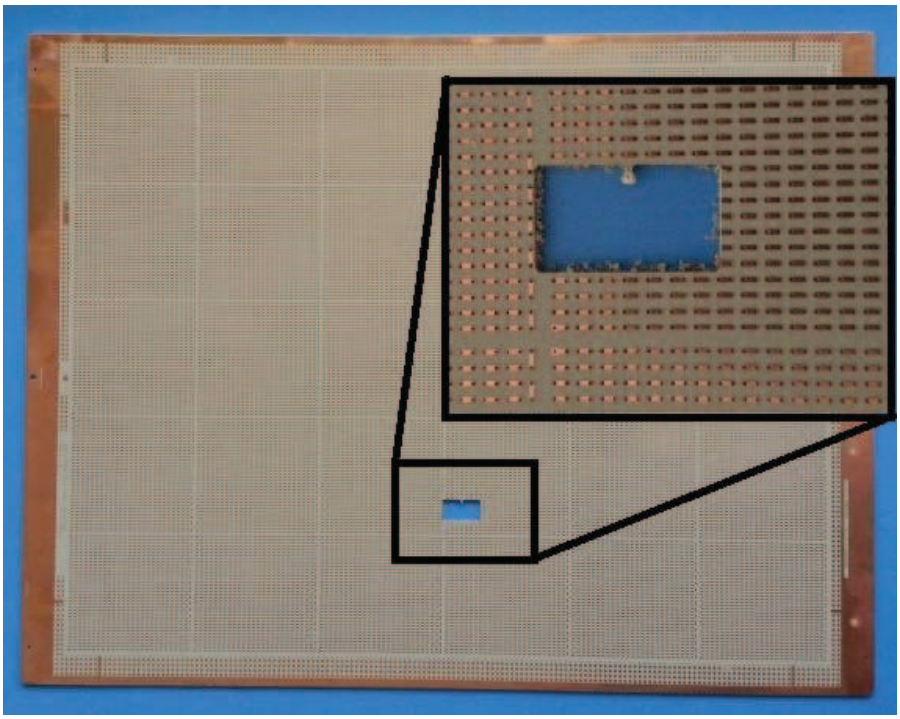


Fig. 3.4: First Daisy chain test on a laminate of Taconic RF-35A2 machined with standard parameters. In detail the withdrawal of the sample analyzed

From the test emerged critical issues regarding the metalization of the holes. In particular, the material residues that have been observed during the preliminary drilling test (Figure 3.2), caused a lack of metalization in the transition between the laminate copper foil and the copper deposited inside the holes (Figures 3.5 and 3.6).
This phenomenon is known as skip plating and it is mainly due to drilling parameters which are not well adjusted for the specific material. However, in some case, the optimization of the drilling parameter can only stem, but not eliminating at all, the skip plating. This is due either to the physical limits of the drilling process and the nature of the material itself.
The iteration of the test abovementioned has allowed the development of the drilling parameters appropriate to the Taconic RF-35A2, such as the entry speed, the angular speed and the chip load.

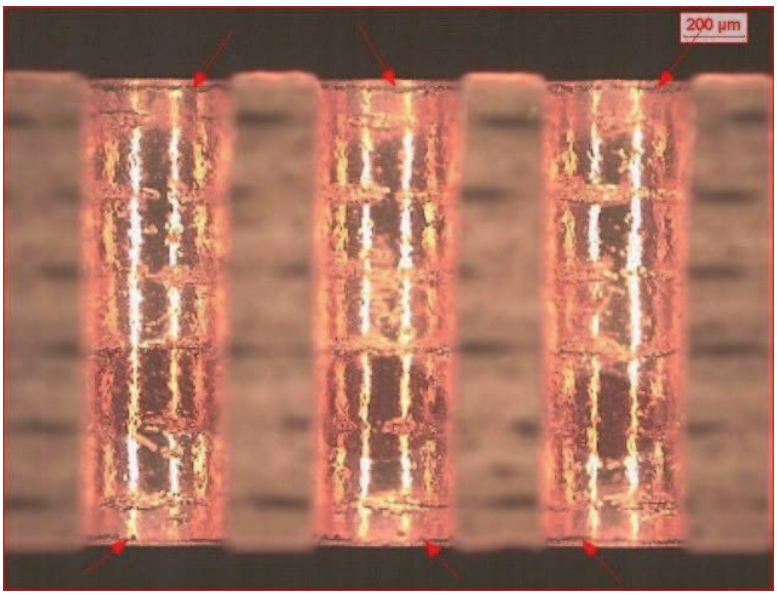


Fig. 3.5: Microsection of opens detected with the Daisy chain test. The red arrows indicate the points of misconnection between the copper foil and the copper deposited inside the holes

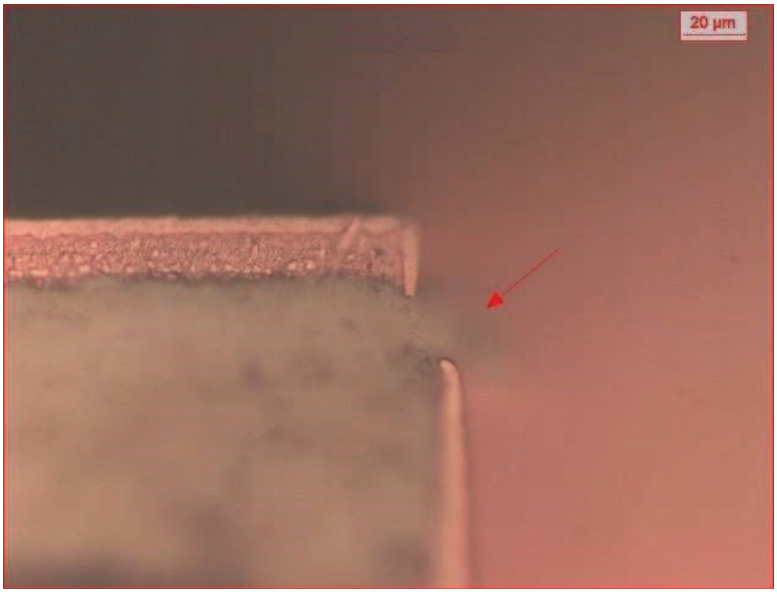


Fig. 3.6: Detail of skip plating

3.1.2. Desmear, electroless and electrolytic panel plating

A tuning of the drilling parameters is a necessary condition to grant the metalization of the holes, but not sufficient. In fact, hole preparation is a critical process in the formation of reliable PTH (plated through holes).
The desmear process, whether based on plasma or on permanganate, or on a combination of the two, is designed to remove any impurities inside the holes and to create a micro-roughening on the resin, enhancing the adhesion of copper that will be subsequently deposited.
Generally speaking, FR4 laminates which are rigid and well drillable, require a simple preparation of the holes that can be achieved with the permanganate only. Conversely, PTFE laminates are soft and suffer from a poor cleaning after the drilling stage. For this reason, an additional preparation of the holes shall be done. As shown, there are two processes that are capable of providing void-free copper plating: the first is based on a sodium-based solution that strips the fluorine atoms from the PTFE molecules, the second is based on plasma etching; the latter one has been chosen for historical reasons.
With the plasma etching, the panels are inserted in a vacuum chamber and gases, like Hydrogen and Nitrogen, are introduced and converted to reactive plasma through a power supply. The plasma reacts at the panel surface (holes included) and the resin smear is removed by a vacuum pump. The advantage of plasma etching is that it is a relative safe procedure. Drawbacks include relatively long cycle times (35 to 60 minutes), and the plasma can keep the treated resin in an inert condition. This condition may lead to metalization issues like plating adhesion failures. A common remedy adopted is to follow plasma desmear with an alkaline permanganate cycle.
The alkaline permanganate process is a multi-step process designed to remove smear and micro-roughen the resin. Moreover, this process is also used to make sure the resin surface is properly prepared in a way that the catalyst and the electroless copper can bond the resin.
The desmear process consists in three main steps: 1) the *Solvent Sweller* swells the resin so that it can be more easily attacked by the permanganate solution that follows; 2) the *Permanganate* solution remove the resin by oxidizing the resin bonds; 3) the *Neutralizer* removes any permanganate remaining on the panel. If the permanganate residuals are left on the panels, these could inhibit catalyst absorption which may cause copper voids along the hole sidewall.
Once the resin in well prepared through the desmearing, the electroless copper can be deposited along the hole wall and the panel surface. The electroless copper is designed to make the holes conductive and allow buildup of electrolytic copper. The electroless copper process involves four key steps: 1) the *Cleaning and Conditioning* is designed to remove soils from the holes and the surface of the panel; 2) the *Micro-etching* micro-roughen the copper surface, improving the bond between the laminate and electroless copper; 3) deposit of *Catalyst* (palladium) on the wall of the hole that will act as an activation site to initiate electroless copper deposition; 4) the *Electroless Copper Bath*, reacting with the palladium, yield copper and, so, the electroless deposition is so completed.
The plating of the electroless copper bath is influenced by many factors, like bath concentration, bath temperature, palladium absorption, but generally, the thickness of copper deposited is in the range 0.3 – 0.7 μm. Such a thickness is then increased by an electrolytic

copper deposition, around 5 µm, to enforce the plating and to make it resistant to the subsequent processes like the micro-etching (etch rate in the range 0.3 – 0.7 µm) used before the dry-film lamination.

Although the metalization process has been defined through successive refinements, the plating of PTFE is critical and not always, a perfect shielding is achieved. To overcome this possibility, a second metalization process is repeated to ensure that the sidewall of the holes is well plated without any copper void that affects the efficiency of the SIW devices will be manufactured with this process. A microsection of a hole on a substrate of Taconic RF-35A2 metallized with the proper process improvements is presented in Figure 3.7.

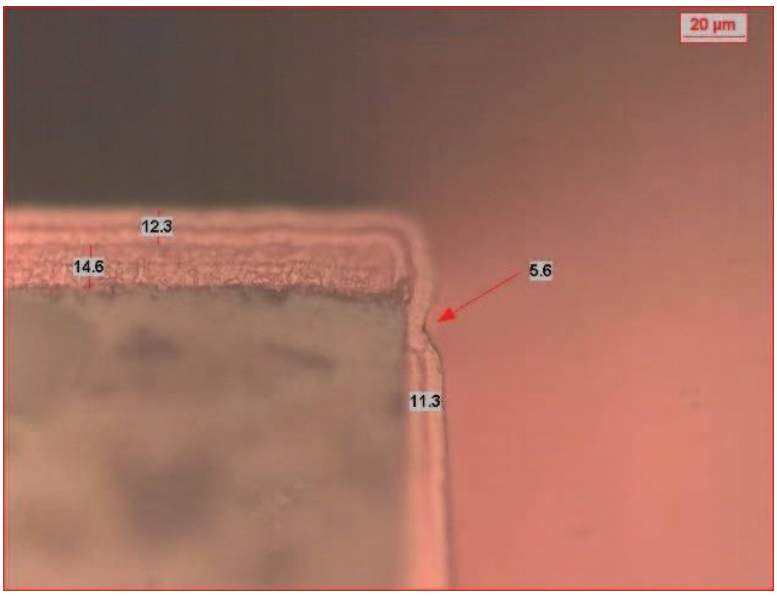


Fig. 3.7: Microsection after the metalization stage. The original laminate copper is 17 µm, reduced down to 14.6 µm after the micro-etching. Each metalization step (2 in total) brings around 6 µm of copper inside the holes and on the panel surface for a total of 12 µm. It can be observed the transition between the laminate and the hole copper, where in a localized area only 5.6 µm are deposited: it would be a copper void in absence of the second metalization step

3.1.3. Imaging

In the scheme pattern plating the dry-film (resist), that is a UV-photosensitive polymer, is laminated onto the panels already metallized with the purpose to realize the external circuit image. The circuit image creation consists in four stages: 1) copper surface preparation, 2) dry-film lamination, 3) image exposition and 4) resist development.

To ensure the adhesion of the film to the copper, the panel surface is treated opportunely, with a mechanical or chemical treatment.
Mechanical treatments foresee the use of brushes based on bristles combined with particles of abrasive materials, such as pumice or Aluminum Oxide Al_2O_3 (abbreviated OxAl), that create a rough copper surface that is desirable for the resist adhesion. An undesirable aftermath on the use of mechanical surface preparation is the distortion (often elongation) of the panel, but it is contained in few tens of PPM (parts per million), that is usually negligible. Conversely, chemical preparations (micro-etching with etch rate of 0.3 – 0.7 µm), leave almost unaltered the dimensionalities of the panels, but could thin the deposit of electroless copper previously deposited. Chemical preparation only, or combined with the mechanical one, is often used when a strong adhesion of the film is required, but at the same time, the deposit of electroless copper inside the holes has to be well verified. A big advantage of the chemical preparation is that it involves a rougher, more preferred, surface than brushes.
As it was pointed out in the previous paragraph, the metalization of holes realized on PTFE laminates is critical, and to preserve it, a mechanical preparation was chosen to laminate the dry-film. In Figure 3.8 it is reported an AFM-STM (Atomic Force Microscope with Scanning Tunneling Microscope technique) of a panel of Taconic RF-35A2 prepared with Aluminum Oxide, significant parameters of this measurements are collected in Table 3.1.

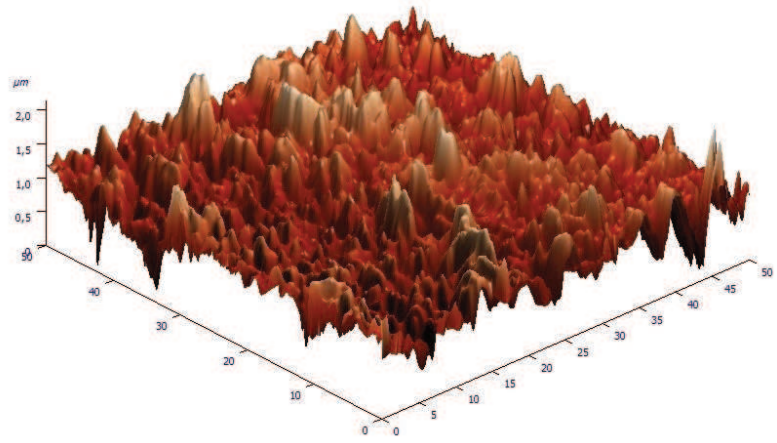


Fig. 3.8: Surface structure after processing with Aluminum Oxide cleaning

Amount of sampling	65536
Measurement window	50 x 50 µm
Peak-to-peak, Sy	2143.94 nm
Ten point height, Sz	1021.56 nm
Average	1044.89 nm
Average Roughness, Sa	188.889 nm
Second moment	10.73.17
Root Mean Square, Sq	244.733 nm
Surface skewness, Ssk	0.114674
Coefficient of Kurtosis, Ska	0.698965

Tab. 3.1: Roughness parameters of a laminate of Taconic RF-35A2 prepared with OxAl

The resist is then applied through a hot roll laminator, where the heat is applied to the pushing rolls and transferred to the interface copper/resist to obtain good conformation of the resist over the panel. Board temperature and the rolls pressure are parameters that have to be calibrated to obtain a good lamination without getting into trouble, notably avoiding resist wrinkling.

The thickness of the dry-film has to be chosen according to the accuracy of the pattern that has to be imaged and the thickness of the copper that will be deposited after. With thin film a better definition of the tracks can be achieved, but at the same time, the thickness of the film has to be enough to host the electrodeposited copper and tin without overhanging (overplating). As it is expected to deposit around 25 µm of copper in the electrolytic line, in order to grant a perfect shielding of SIW devices will be realized, a dry-film 40 µm thick was used. The thickness 40 µm was assessed as the best tradeoff between pattern accuracy and copper deposit, for this specific application.

The exposure of the dry-film for outer layers is done in negative. This means that the photopolimerization, obtained by radiating a certain dose of UV-light over the dry-film, involves only areas which are complementary to the final image.
The exposure is done digitally; the circuit image is rasterized in a matrix, where each cell is a pixel of the pattern with a size of 2 µm. The expositor used is equipped with a multi-wavelength light source (LED radiation with peaks at 375 and 405 nm) that ensures a complete polymerization of the film, from the interface with the copper to the top surface.

The negative image realized with the dry-film, will impede to the electrolytic copper to be deposited over the laminate, while the dry-film non-polymerized will be dissolved through a bath of $NaCO_3$, discovering in this way the pattern to be accrete.

3.1.4. Electrolytic pattern plating

The aim of the electrolytic pattern plating is to increase the copper deposit, inside the holes and on the surface, already deposited with the electroless line and uncovered from the dry-film. Typical copper deposits are around 25 µm, but theoretically, any thickness can be obtained (it depends mainly on the density of current, concentration of bath and immersion time), providing the appropriate thickness of dry-film. Another fundamental operation done in the electrolytic line is the deposit of a subtle layer of Tin over the copper (named etch-resist), in order to protect the circuit image during the etching phase.

A basic scheme of the electrolytic cell is presented in Figure 3.9. Here, the panels are inserted in a sulfuric acid copper bath, composed by copper sulfate, sulfuric acid, levelers, brighteners and water. During the electroplating, the ion concentration is kept constant by dissolving copper tokens in the electrolyte. The deposition of copper on the top and bottom surfaces of the PCB is obtained through a redox reaction stimulated by electric current (voltage generators):

Cathodic reaction (reduction) $Cu^{2+} + 2e^- \rightarrow Cu_{(s)}$

Anodic reaction (oxidation) $Cu_{(s)} \rightarrow Cu^{2+} + 2e^-$

On the PCB surfaces and inside the its holes, the cations (Cu^{2+}) get the electrons ($2e^-$) from the anodes and they are transformed in metal atoms ($Cu_{(s)}$). In this way, a subtle layer of copper gradually covers the cathode, while the anode is slightly thin releasing Cu ions in solution.

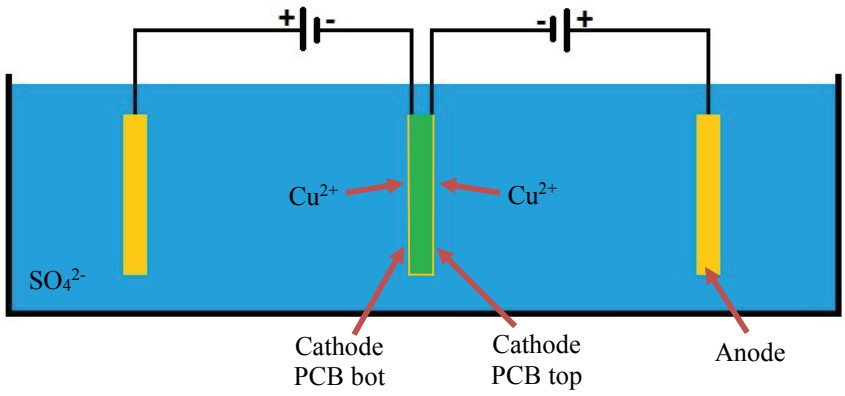


Fig. 3.9: Basic scheme of a typical electrolytic cell

The deposit of copper shall be enough to guarantee a good shielding of the devices. The skin depth for the copper at the frequency of 10.7 GHz (lowest frequency of the DVB-S spectrum) is:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0}} = \sqrt{\frac{1.68E-8}{\pi(10.7E9)(4\pi E-7)}} \cong 1.5\ \mu m \qquad (3.1)$$

The meaning of δ, is that at a distance of 1.5 µm from the interface dielectric-copper toward the external region, the electric field is attenuated of a factor 1/e. A deposit of copper equal to 5δ = 7.5 µm will attenuate the electric field of a factor exp(-5) = 0.0067. Therefore, copper thickness higher than 7.5 µm will grant that the radiated electric field through the copper will be lower than the 1% of the internal field.

As the copper deposit on a panel placed inside the electrolytic cell is not uniform because the density of current is not uniform (it depends on position of the panels, pattern, bath concentration, deposition velocity and others), an extra deposit has been foreseen to be sure that in all the holes at least 10 µm of copper are present. From a metallographic microsection (Figure 3.10), it has been verified this condition, that is widely respected.

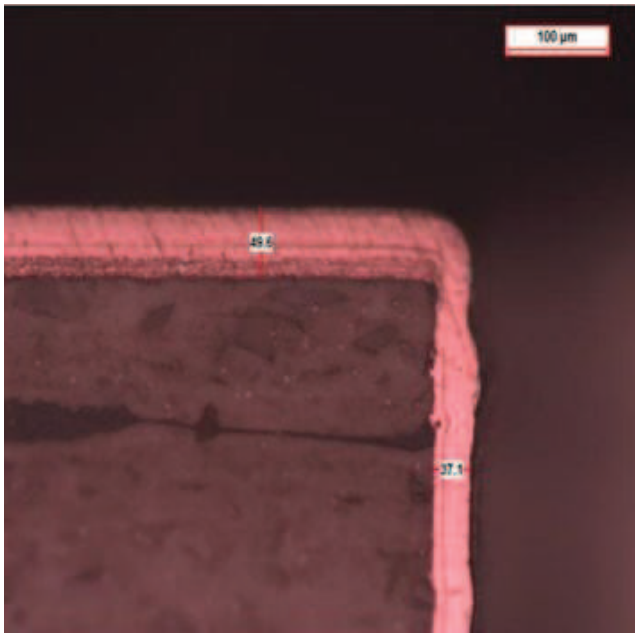


Fig. 3.10: Microsection of a hole after the electrolytic line. Inside the holes the deposit of copper is around 37 µm, while on the external surface copper thickness is almost 50 µm

3.1.5. SES (Strip, Etch and Strip)

The acronym SES encloses in it three different stages that bring the half-processed PCB in a form almost completed. These three stages are composed by the Stripping of the polymerized dry-film, the Etching of the copper in excess and the Stripping of the tin with function of etch-resist.
The panel after the electrolytic line presents areas where the copper has been grown (complementary to the dry-film) that are not directly visible because covered with tin and areas under the dry film where only the laminate and the electroless copper are present.
The stripping of the dry-film has the purpose to discover the laminate and electroless copper that will be successively etched. Conversely, in the etching stage, the upper circuit image is protected by the tin while its lateral sides are not. Due to the lateral etching, the size of the pattern will be reduced, roughly in a ratio 1:2 laterally to down. E.g. track width imaged = 100 µm with laminate + electroless copper = 20 µm, after the etching the track width will be 80 µm, because it has been reduced of 10 µm per side.

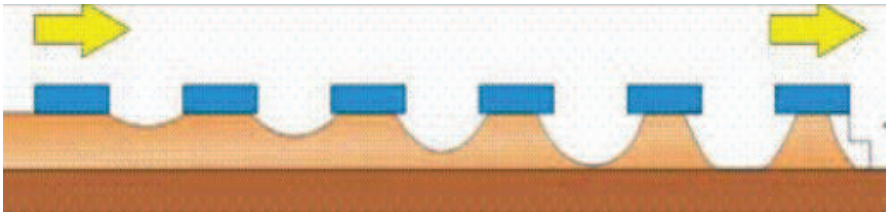


Fig. 3.11: Pattern shrinkage due to the lateral etching. The yellow arrows represent the etching direction, while the blue boxes represent the tin (etch-resist)

To compensate the phenomenon of the lateral etching, the circuit image is previously enlarged, this operation is known as “etch compensation”.
Unfortunately, the ratio 1:2 abovementioned is only theoretical, and in practice, it depends on many factors, all of them attributable to the behavior of the etching liquid.

The main factors that affects the lateral etching are:

1) Immersion time, and then the line speed, in the alkaline etching solution. The longer time the panels are immersed in the etching solution and the more the lateral etching will be accentuated. The speed of the line has to be enough low to etch all the laminate and electroless copper, but at the same time, enough quick to prevent the pattern undercut.
2) The orientation of the panel inside the etching line and the arrangement of the PCBs within the panel. The etch rate varies from the top to the bottom and from the center to the edges of the panel. This effect is known as “puddling effect”: it causes a slower etch rate near the center of the top side due to the liquid buildup, while on the bottom it is less evident because the gravity run-off the liquid.

3) Pattern density in the circuit. Areas of circuits very dense of tracks and pads will reduce the etch rate due to the saturation of the etching liquid, conversely, isolated features will be subjected to high etch rate thanks to the efficiency of the liquid.
4) The presence of big holes inside the circuit. As the point 3), whereas the etching liquid can be renewed, the etch factor will be increased.
5) Copper content. Copper concentration affects the etch rate, this means that the etching is not constant over the time.

Now, the image compensations and the speed of the line are based on the experience of the operators, but some companies are working on software to predict the exact etch compensation to be applied in each point of the panel.
The compensation of all the factors that influences the etching is fundamental especially in high frequency and impedance controlled applications, where the dimensionality of the pattern strongly influences the functionality of the devices so realized.

Chapter 4.

Prototype design and development

In Chapter 3, it was presented the production process for the correct implementation of componentry SIW in Taconic RF-35A2. The research project provides, in addition to the realization of a planar antenna for the reception of DVB-S, also a number of passive devices such as directional couplers, power dividers and transitions.
Large part of the treatise is dedicated to the presentation of elementary radiators. These radiators will be arranged in a rank in order to achieve a sufficient gain to satisfy the specifications.

4.1. SMA to SIW transitions

An accurate characterization of packaged microwave circuits, require planar transitions with a low return loss all over the bandwidth of interest. A good candidate for interface the SIW components to the measurement equipment is the SMA connector, a compact coaxial RF connector designed to operate from DC to 18GHz.
In literature there are present many transitions from RF connectors to SIW components, but a large part of them is substantially microstrip to SIW transitions and the connector is soldered in the microstrip end. One of the most attractive characteristics is the absence of parasitic radiation outside the device. A microstrip-based transition could nullify this advantage. To remain coherent to the SIW philosophy, two different self-shielding transitions are designed and developed.

4.1.1. Two ports transition

The first transition treated is a SIW version of the classical coaxial-waveguide transition. To realize a closed structure, which guarantee the shielding, a SMA connector is placed in the middle of a transmission line with the central conductor penetrating orthogonally the substrate [28]. In this way a 3-port junction (with low losses) is realized and as it is well known that it cannot be matched at all the three ports. It was decided to share the reflection towards the three ports and close one of these ports on a reactive load, a short for instance. As the three-port junction so realized is symmetrical, also the reflection coefficient to the relative ports will be the same. To achieve the same reflection, the only parameter to be adjusted is the width of the guide. Through the simulator HFSS, the width of the guide has been varied up to the reflection at the SMA and one of the two port of the guide was the same at the frequency of mid-band that is f_0 = 11.7 GHz. The width of the guide, that permits to verify this condition is 13.9 mm (from the center of the vias). A sketch of the transition is shown in Figure 4.1.

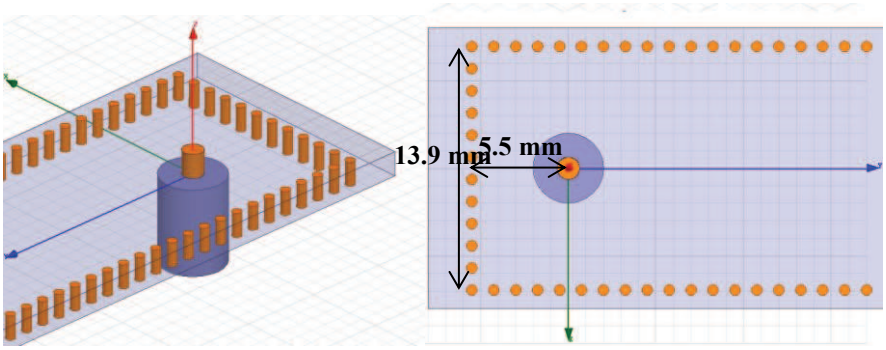


Fig. 4.1: Sketch of the transition, a 45° view on the left and a top view on the right

The distance "l" to place the short from the coaxial, in order to guarantee a perfect matching at the coaxial port, is given by the formula:

$$l = \frac{1}{2j\beta_2(f_0)} \ln\left(-\frac{s_{33}^* \Delta s}{s_{11}}\Big|_{f=f_0}\right) \pm \frac{k\pi}{\beta(f_0)} \qquad (4.1)$$

Where:

- S_{11} is the reflection coefficient at the SIW port opposite to the short circuits;
- S_{33} is the reflection coefficient at the coaxial port;
- β_2 is the propagation constant in the SIW;
- Δs is the determinant of the original 3-port junction (with no reactive element).

A successive fine tuning, was performed, by varying the distance l in the electromagnetic simulator, in this way, a better matching to the two ports was achieved.
The pitch of the vias equal to 1.25 mm and their diameter equal to 0.6 mm were chosen according to (1.2), these conditions permit a perfect equivalence with the DFW.
.
As shown in Figure 4.2, a return loss of 15 dB all over the band 10.7 GHz – 12.7 GHz. This permits a good matching of the devices. Unfortunately, with this configuration it was impossible to obtain a better matching, due to the wide band (2 GHz, FBW = 17%) to cover.

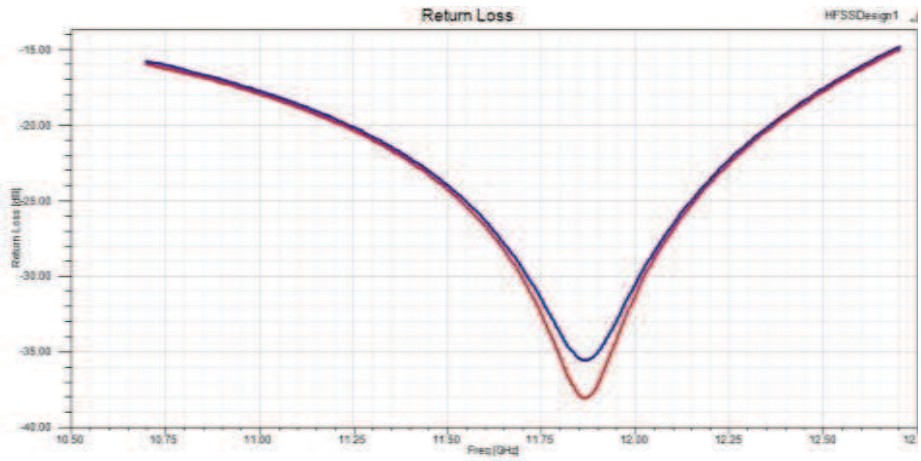


Fig. 4.2: Reflection coefficients of a 2-port transition SMA-SIW. Red and blue line are relative to the SIW and coaxial port respectively

4.1.2. Three ports transition

With the same methodology used in 4.1.1, it has been possible to design a 3-port SMA-SIW transition. Such transition could be used as the main node in a corporate feed line. In this case the design is easier because the only parameter to be tuned is, again, the width of the guide. Even here the width of the guide was chosen in order to share the same reflection toward the three ports. As expected, in the case of a three port junction, the return loss will be higher respect the case of a two ports. The reflection coefficients for this type of junction is shown in Figure 4.3.

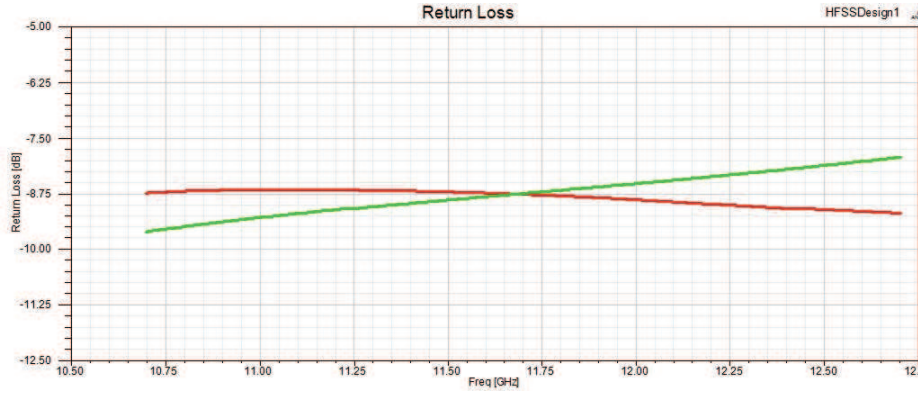


Fig. 4.3: Reflection coefficients of a 3 port transition SMA-SIW. Red and green lines are relative to the coaxial and SIWs (equal for symmetry) ports respectively

4.2. Transmission line

A segment of transmission line, is the root element from which all the other elements will be derived. Theoretically, under the conditions of perfect dielectric ($D_f = 0$) and conductor with an infinite conductibility ($\sigma = \infty$), the magnitude of the fields related to the waves travelling inside the guide are unaffected and their phase changes according to the propagation constant and the length of the segment. Instead, in the case of real dielectrics and conductors, part of the electromagnetic energy is dissipated from the conductor and the dielectric, furthermore in SIW technology a minimum amount of energy is irradiated through the holes, but this is generally negligible compared with the other two causes.

To dimension a waveguide it is sufficient to impose a certain width of the guide in a such a way that the unique mode in propagation is its fundamental. For a DFW filled with a material with relative permittivity of ε_r, the cutoff frequency of the TE_{10} is:

$$f_{c10} = \frac{c_0}{2a\sqrt{\varepsilon_r}} \qquad (4.2)$$

To obtain the condition of mono-modality and to keep the dispersion contained, the width of the guide "a" must be: $f_{min} > 1.3 f_{c10}$ and $f_{max} < 2 f_{c10}$, where f_{min} and f_{max} are the minimum and the maximum frequency of interest. Reversing the formula (4.2) and applying the two conditions already given, it can be written:

$$5.7\ mm = \frac{c_0}{2 \cdot 1.3 f_{min}\sqrt{\varepsilon_r}} < a < \frac{c_0}{f_{max}\sqrt{\varepsilon_r}} = 12.62\ mm \qquad (4.3)$$

With f_{min} = 10.7 GHz, f_{max} = 12.7 GHz and $\varepsilon_r = 3.5$.

It was chosen arbitrary a width of 10.5 mm corresponding to a width of the corresponding SIW structure (1.2) equal to 10.8 mm, having chosen according to (1.4) and (1.5) the pitch and the diameter of the vias equal to 1.25 mm and 0.6 mm respectively. A guide long 109 mm (from the center of SMAs) was simulated and the model is presented in Figure 4.4.

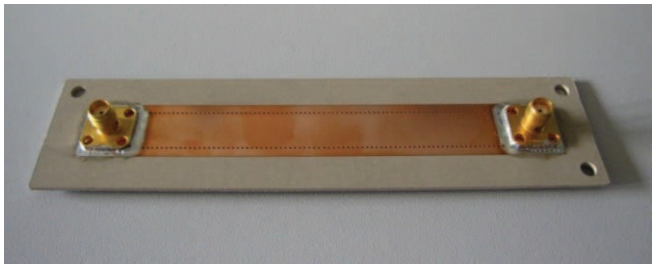


Fig. 4.4: A segment long 109 mm of a SIW transmission line. At the end of the guide are present the two transitions with the SMA

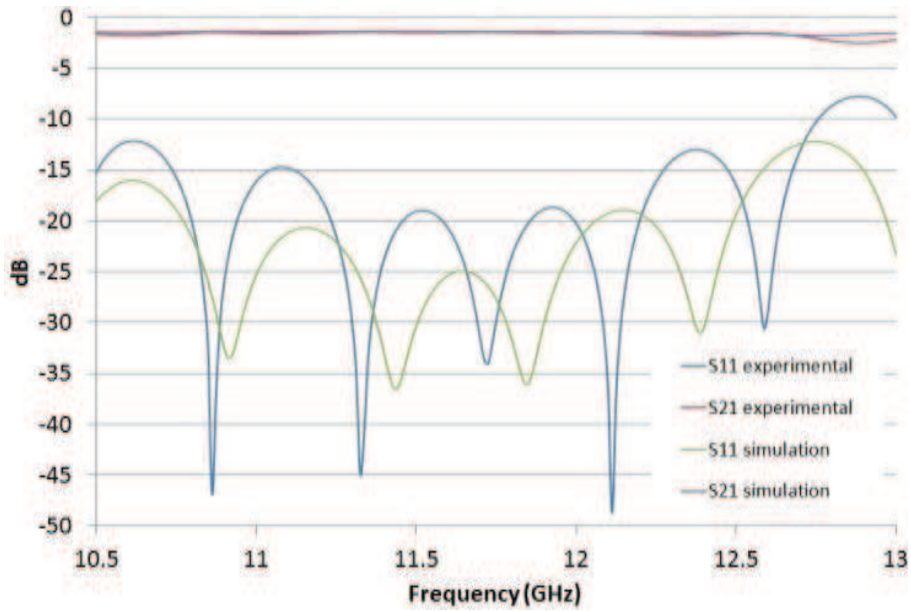


Fig. 4.5: Comparison between simulation and measurement of a segment of SIW in Taconic RF-35A2 long 109 mm

The graph shows an excellent superposition between simulations and measurements, especially at frequencies for which there is a good matching with the ports. For the simulations were used D_k = 3.48 and D_f = 0.0038, according to the dielectric constant characterization (cfr. 2.2.1.3). Preliminary simulations performed with nominal material parameters (D_k = 3.5 and D_f = 0.0015), present better performances, in particular the transmission coefficient is about 1 dB more optimistic respect the real case. These measures confirm that the substrate is affected from an additional loss factor that has to be taken into account to reproduce more closely the devices simulated.
The transmission coefficient is constant with the frequency and equal to -2 dB. This value encloses ohmic and dielectric losses.

4.3. Power divider

A very important role in the realization of an antenna array is covered by the network for the signal distribution. In the case of a receiving antenna, it allows conveying the signal sensed by the slot towards a single point. Vice versa, in the case of a transmitting antenna, from a single point it is possible to feed each slot with appropriate amplitudes and phases.
It is proven [29], that the maximum gain of an antenna is given from the uniform distribution. With the uniform distribution, it is possible to obtain a main lobe in the boresight direction and secondary lobes with a gain of -13.5 dB compared to the maximum. To achieve such a

distribution, the easiest way is to realize a corporate feed network, that is composed of a series of balanced power dividers (equiamplitude condition) interconnected by section of transmission line of a fixed length (equiphase condition).
In this perspective, the power dividers have to guarantee a good matching between the ports and to ensure the maximum signal transmission between the input and the radiating elements. In this paragraph, a 3 port power splitter is presented.

A balanced power splitter consists of a three ports junction. In Figure 4.6 we can find a first prototype of the power divider, in which are noticeable three fundamental parts:

A. a septum, symmetric compared to the center of the guide 1, facilitates the division of the power through the ports 2, 3;
B. an iris for the matching with the port 1;
C. a λ/4 section to adapt the waveguide wide 10.8 mm with the SMA-transition wide 13.9 mm.

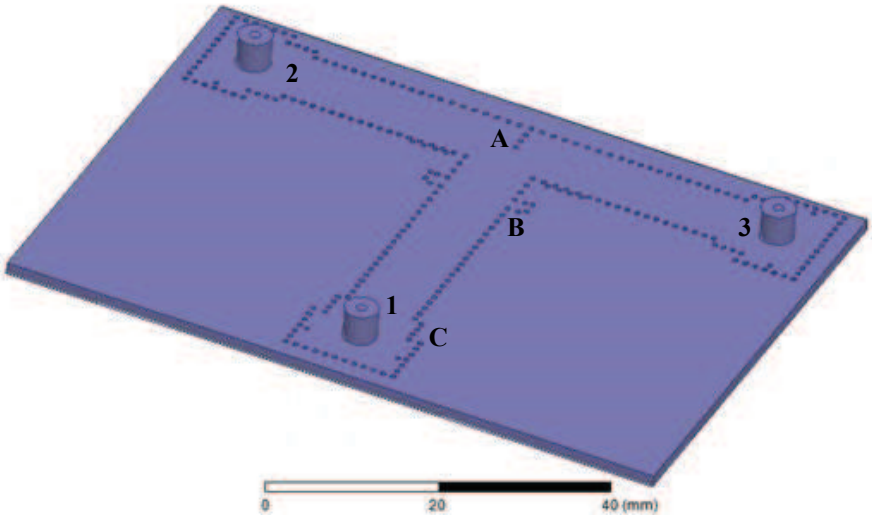


Fig. 4.6: A balanced power divider in SIW technology: A) septum; B) iris; C) λ/4 adapter

As the power splitter over mentioned is a 3 port junction, with low losses, it is impossible to match the three ports simultaneously. For this reason it was decided to match the port 1 with a reactive element, its dimensions were optimized used the electromagnetic simulator. In the same way the shape and the length of the septum were varied, since to obtain a good matching of the port 1 and acceptable adaptation of the other two ports 2 and 3.
The prototype of the power divider was made through the proper process (cfr. 3) and a T-junction so realized is shown in Figure 4.7.

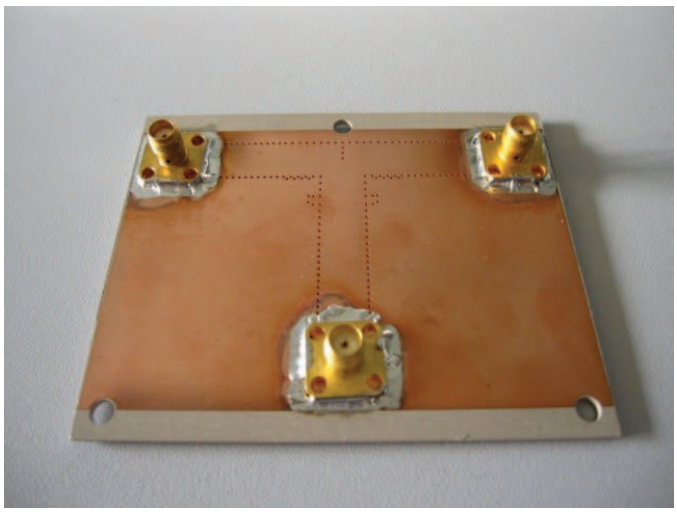


Fig. 4.7: Prototype of a 3dB power divider

A comparison between theoretical and experimental results is shown in Figure 4.8 it shows the relation between the reflection coefficients to the three doors.

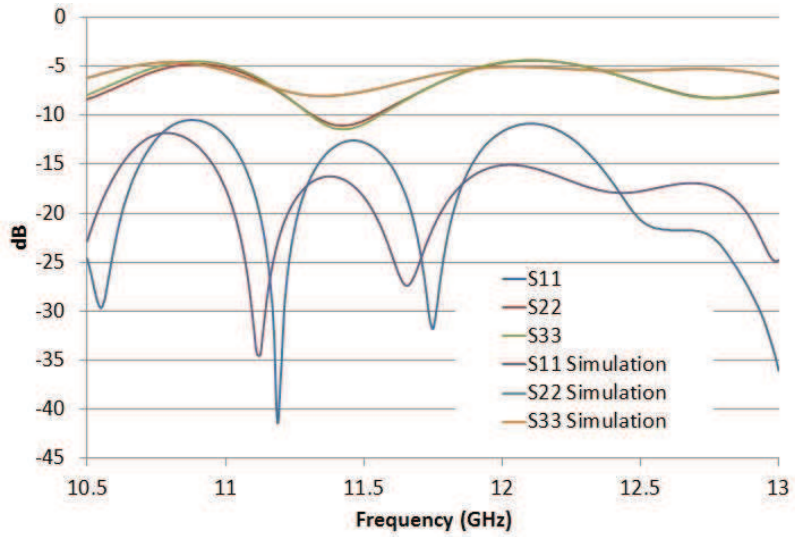


Fig. 4.8: Simulated and measured reflection coefficients

From the analysis of the curves, it can be noted that the adaptation at port 1 is slightly worse respect the simulation. This aspect is attributable to the production tolerances, to the soldering of the connectors and to the deviation of the dielectric constant measured compared to that used in the simulations.

The graph in Figure 4.9 shows the comparison between the transmission coefficient of the same junction.

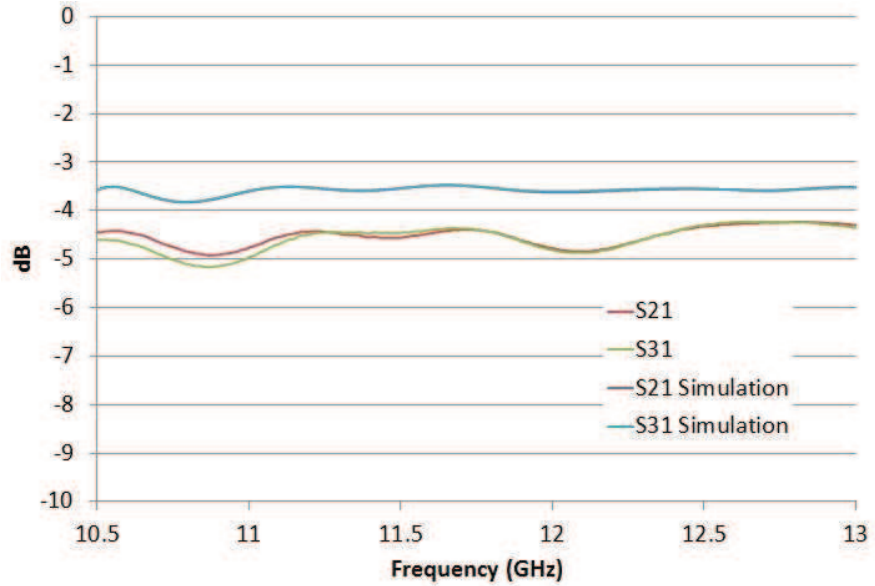


Fig. 4.9: Simulated and measured transmission coefficients

The same considerations done with the comparison of reflection coefficients can be done for the transmission coefficients. Furthermore, at low frequencies the parameter S21 and S31 show a small difference that must be attributable only to construction tolerances, and cannot be amenable to a symmetric device.

Despite the modest performances of the power divider so realized, it results very compact. This property is very suitable for an application of this type, a possible solution to keep the costs contained is to realize the radiating slots and the feed line in the same substrate.
A more flexible solution foresees the disposition of the feed line and the radiating slots in two separate substrates. In this situation the cost for the material becomes double and it appears the problem of the bonding of the two layers.

4.4. Directional couplers

A fundamental component in the microwave networks is the directional coupler. The directional coupler permits to direct a certain part of the power travelling into the main guide in a secondary guide, named coupled guide. The amplitude and the phase of the signal in the coupled guide depend substantially on the coupling mechanism between the two guides.
The use of a directional coupler respect a power divider can be preferred because it is possible to match the four (or more) ports at the same time, this makes it particularly suitable in the beam forming networks.

4.4.1. Four ports coupler

A four ports directional coupler can be used as a power splitter if one of the ports is closed in a matched load, moreover to obtain a uniform corporate feed network, all the nodes should be balanced divisors, such as in the case of a 3dB directional coupler.

A simple power divider can be designed by realizing an aperture between two parallel waveguides. In first instance, in order to facilitate the design of the coupler, the guides realizing the coupler are considered as DFWs with full metallized walls and only in a second moment, the vias will be introduced to constitute the lateral walls.
In the device like that shown in Figure 4.10, with two symmetry planes respect XZ and YZ, the signals coming from the direct port (2) and coupled port (3) are in quadrature of phase, if the matching of all the ports is guaranteed. The reciprocity condition and the absence of losses guarantee that one of the ports is insulated respect the others (4). Obviously, because the dielectric substrate is lossy, is not possible to obtain a perfect insulation of one port and an exact difference of phase between the direct and the coupled port.

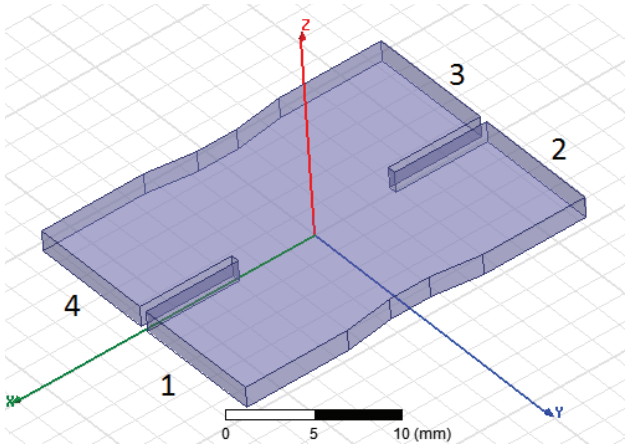


Fig. 4.10: Conceptual design of the directional coupler with the numbering of the ports

The parameters used in the synthesis of such a coupler are the width of the aperture and the dimensions of trapezoid inside each guide. The first determines the coupling between the guides, instead the shrinkage trapezoid shaped is used to tune the matching.

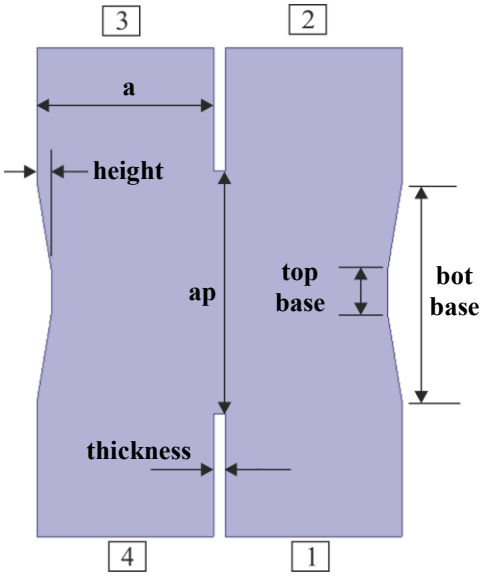


Fig. 4.11: Degrees of freedom of the directional coupler proposed

Furthermore, thanks to the symmetry of such a device, it is possible to use an odd/even analysis to simplify its synthesis, by dividing the device in two less complex devices. Each analysis is performed by imposing different boundary conditions in the plane of symmetry (longitudinal axe), that are the condition of magnetic wall for the even case and electric wall for the odd case. The sub-devices so obtained are solved separately, through the use of the electromagnetic simulator HFSS. Acting on the parameters abovementioned, it was possible to obtain a 90° of difference between the direct and the coupled port that has as subsequent an equal division of the power between the ports 1 and 2.

Parameter	Description	Value [mm]
a	Broad side of the guide	10.25
b	Narrow side of the guide	1.52
ap	Length of the aperture between the two guides	13.352
top base	Top base of the trapezoidal tune element	14.264
bot base	Bottom base of the trapezoidal tune element	3.455
height	Height of the trapezoidal tune element	1.522
thickness	Distance between the two guides	0.6

Tab. 4.1: Geometric parameters of the 4 ports coupler

Starting from the synthesis of the DFW directional coupler, it is possible to replace the lateral walls through rows of metallized vias, following the equivalence rules for the SIWs (cfr. 1). The prototype so designed was realized (Figure 4.12) and measured.

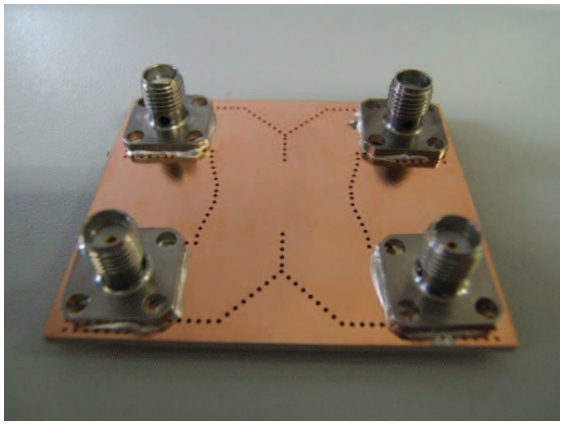


Fig. 4.12: Prototype of a 3dB directional coupler

The experimental results (Figure 4.13) show a balanced behaviour of the transmission coefficients up to 12.5 GHz, the matching and the insulation are greater than 15 dB.

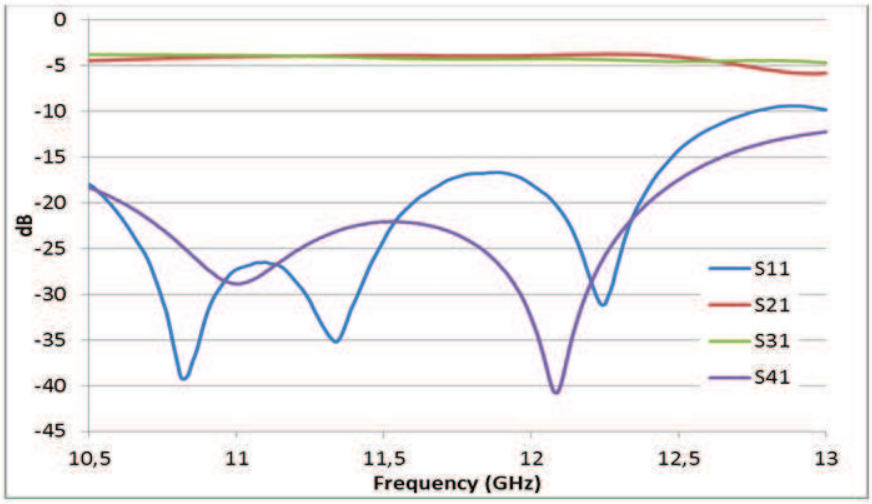


Fig. 4.13: Experimental S-parameters of the 4 ports directional coupler

The difference of phase between the ports 2 and 3 is closed to 92° with a maximum deviation of 2° all over the bandwidth as shown in Figure 4.14.

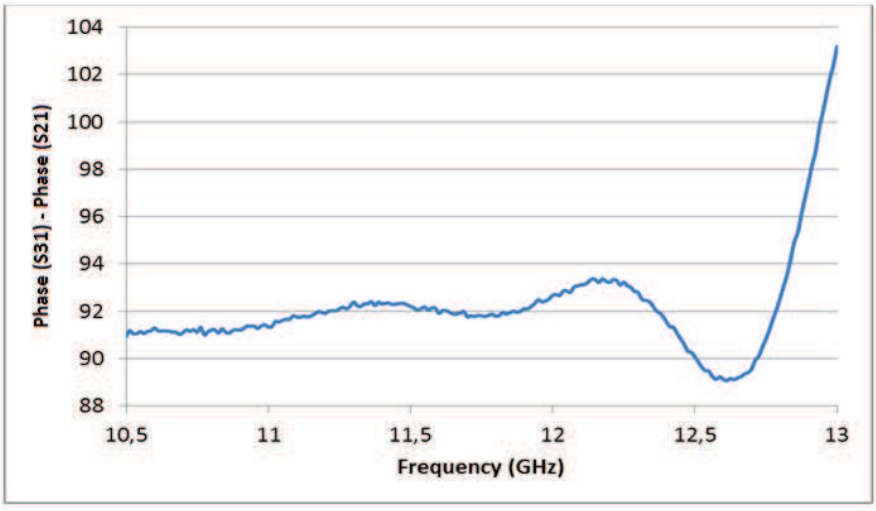


Fig. 4.14: Difference of phase between the direct and the coupled ports

Finally, the losses of the directional coupler are estimated at the frequency of 11.25 GHz, where $|S_{21}| = |S_{31}|$.

$$I.L. = 10\log\left(\frac{P_{in}}{P_{out}}\right) = 10\log(|S_{21}|^2 + |S_{31}|^2) = 0.89\ dB \qquad (4.4)$$

A complete description of the abovementioned four ports directional coupler can be found in the paper of Venanzoni et al [30].

4.4.2. Six ports coupler

A six ports directional coupler is less common respect a four ports, but can be used for the same purpose. Under a theoretical point of view, a reciprocal and lossless six ports device that is matched at all the ports, will imply that two of the ports will be insulated and the coupling coefficients will depend on the geometry of the coupler itself.
In order to use the devices here proposed as a base for a feed line of a planar and uniform array, the intention is to use a six ports directional coupler like a balanced three ways beam splitter with all the ports matched.
Once again, the use of directional couplers is preferable to avoid undesired mismatching losses that degrade the response of the antennas connected under a point of view of the signal

to noise ratio and the radiation pattern. On the other hand, the use of directional couplers foresee a number of ports not directly used, which are closed on the matched loads. This involves an increase of the size of the components, which is in contrast with the SIW philosophy.

In literature there are several directional coupler designs, that can be assembled in two categories:

1) Six ports directional couplers realized through the combination of basic four ports directional couplers and line sections;
2) Six ports directional couplers realized as a unique block.

The advantage of the first group is that these couplers are relatively easy to design, because it is possible to reduce the design to different less-complex devices, on the other hand these couplers are bulky. Conversely the couplers belonging to the second group, although they are more complex to design because of the higher number of variables, they are more compact and generally have broad bands.
The devices here treated, are inspired on the paper of Alessandri et al [31], because they have high performances, they are compact and are orientated to be implemented in SIW technology.

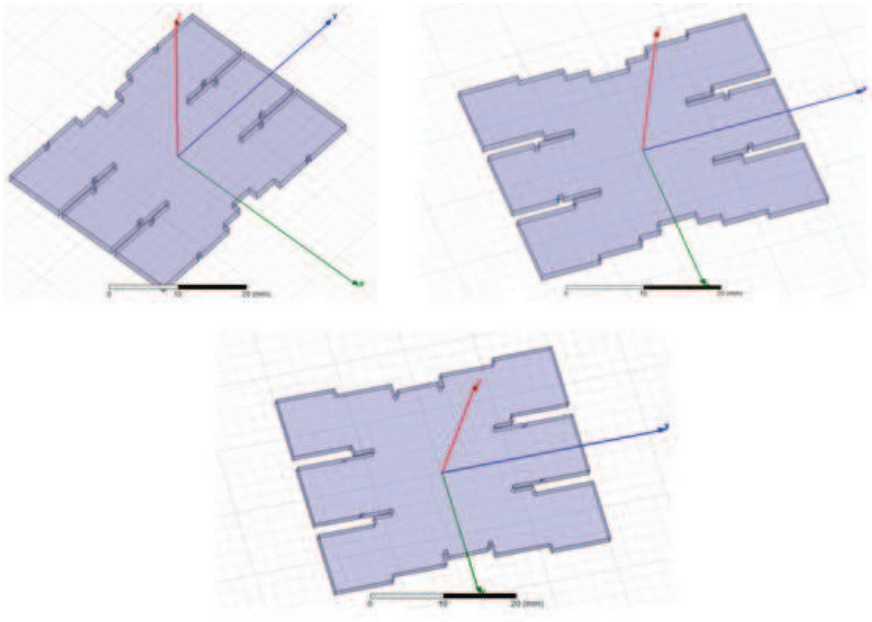


Fig. 4.15: Three different schemes for the six ports directional coupler

Substantially, the three devices shown in Figure 4.15, differ only for the matching stages that are composed of steps and irises. Also in this case is it possible to exploit the symmetry of the device to simplify its synthesis. The structure taken into account is shown in Figure 4.16.

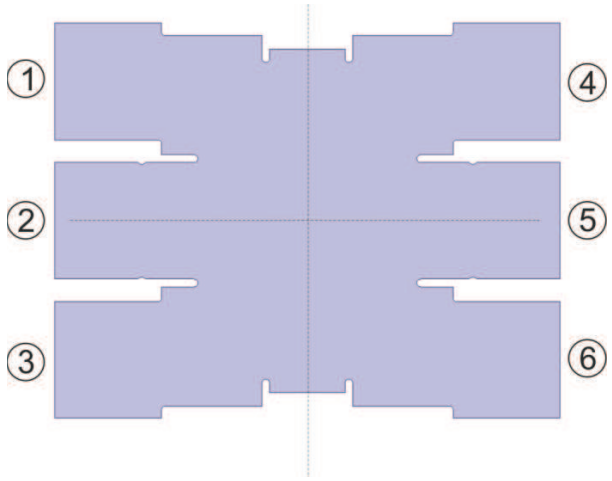


Fig. 4.16: The six ports directional coupler structure with the numbering of the ports and the two plane of symmetry (dash lines)

Thanks to the symmetry it is possible to impose the following equalities of the S-parameters:

- $S_{11} = S_{33} = S_{44} = S_{66}$;
- $S_{22} = S_{55}$;
- $S_{12} = S_{32}$;
- $S_{42} = S_{62}$.

This devices is designed to obtain an equal division of the power through the three ports in one side (1,2,3 or 4,5,6) when only one port of the opposite side is supplied, the remaining two ports will be insulated.
The design method of the six ports directional coupler follows that used for the equivalent four ports, but with much more degrees of freedom represented from the matching stages as well as the aperture that determine the coupling. Even in this case, the project starts from the equivalent device in DFW, and at the end the vias takes place of the lateral walls and a SMA to SIW transition is placed in each port to characterize the device (Figure 4.17).
Such a device was simulated and the S-parameters are reported in the Figures 4.18 and 4.19. From the graphs can be noticed a flat response in the band 10.5 – 12.5 GHz can be noticed, with a matching better than 15 dB.

A complete description of this device is reported in the paper of Venanzoni et al [32].

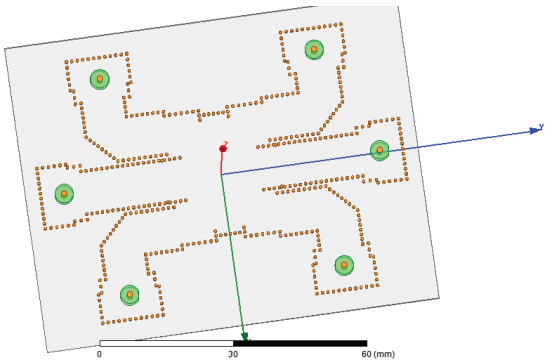
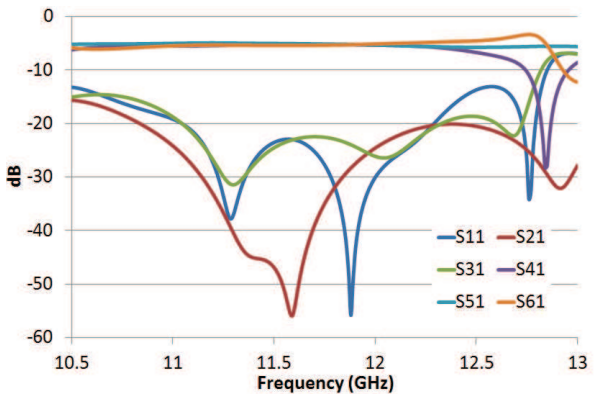
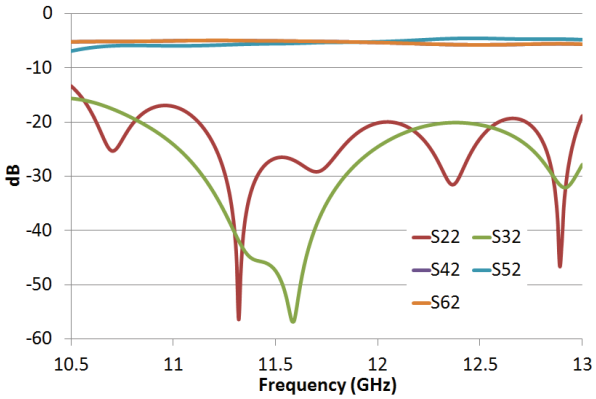


Fig. 4.17: Six ports directional coupler in SIW technology with the transitions for the connectors



a)



b)

Fig. 4.18: S-parameters related to the port 1 (a) and to the port 2 (b)

4.5. Antenna

The main goal of the project is the development of an antenna in SIW technologies with performances comparable to the standard TV dishes used to receive the DVB-S (Digital Video Broadcasting Satellite) signal. Having to have similar capabilities to the parabolic antennas, the minimum gain to be achieved in this context is around the 25 dB. Such a gain cannot be obtained with a single element, but with a rank of elementary radiators supplied with equal magnitude and equal phase, the array so formed is a planar and uniform array which guarantees the maximum gain respect the area of the antenna.
A fundamental aspect of this antenna is the huge band to be covered. The DVB-S signal has 2 GHz of bandwidth, the design of the antenna has to take into account also this aspect. Because each elementary radiator can be represented with a network of lumped element, the response of these elements strongly depends on the frequency, then also the behaviour of the radiators has a dependency on the frequency. The design has to minimize this effect in order to keep the properties (gain, boresight and return loss) of the antenna as much constant as possible over the band. Moreover, to maximise the spectral allocation, the DVB-S signal is composed of two orthogonal and interleaved signals, the receiving antenna shall be designed to distinguish both signals and to make sure that each signal does not interfere with the others. These properties suggest the use of two slotted sub-antennas with an offset of 90° between them, the use of the slots generally guarantees also a low cross-polarization coupling that is suitable for this type of application.
The SIW technology implies the use of dielectric substrates that are lossy. To minimize the losses, and hence to maximize the gain of the antenna, RF materials shall be used. A second aspect regards the space optimization over the dielectric laminate: because the RF materials are expansive and to keep the cost of the antenna competitive, the volume of material and the scrap should be minimized. A solution is to use the substrate to host either the elementary radiators and the feed line that interconnect them. The latter is satisfied if the material chosen has a sufficient high Dk, but this is contrary with the losses. Generally, dense materials with high Dk (e.g. ITEQ IT180 Dk=4.70, Df=0.018) have also high losses, instead soft materials with low Dk (e.g. Duroid 5880 Dk=2.20, Df=0.0009) have also low losses.
Finally yet importantly, the design of such antenna must take into account the physical feasibility, which is given by the physiologic limitations of the manufacturing process; furthermore, the design should make the manufacturing process as easier and linear as possible to minimize the industrial costs and to prepare, in case of success, the prototype to the mass production.
All the motivations above mentioned make this antenna a very challenge project, which is proven to the fact that nothing of similar exists on the market.

4.5.1. Elementary radiators

Classical slotted antennas are still widely used in many applications as they often represent the best trade-off between cost and performances; for the SIW slotted antennas the cost is lower even if a physiological reduction of the performances is appreciable.
The slotted antenna have a series of advantage respect the parabolic antennas beyond the others: a lightweight and more compact mechanical structure, absence of disturbs due to the "Spill-over" or "Back-radiation" and a better control of the distribution of the excitations on the apertures. Moreover, also in the planar form, the slots are preferred to the patches because their inherently narrow impedance bandwidth.
The bandwidth of an array of slots is sufficiently wide, if the number of the aperture is low, in fact, each aperture can be represented as a reactive load that reflects backward part of the energy coming from the generator. If the number of the slots is high, all the contributions due to the reflections of slots sum, this involves a strong limitations in the bandwidth.
The latter model suggests to keep much low as possible the number of radiators supplied from each branch, even if the feed line becomes more complex.
In order, these slot radiates have to be placed in a way to interrupt the surface current lines circulating on the internal walls of the guide that support the mode TE_{10}. For a classical waveguide the line of currents are shown in Figure 4.19.

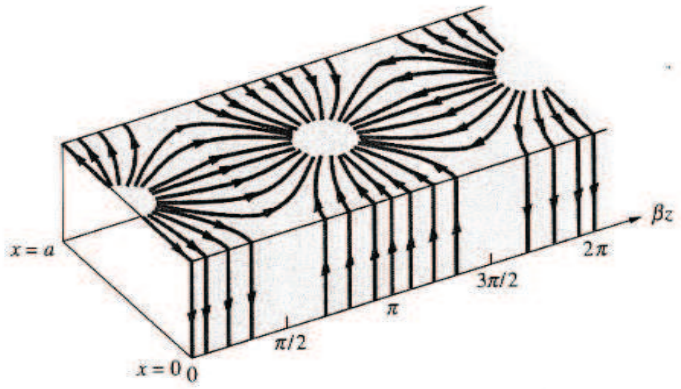


Fig. 4.19: Surface current of a waveguide with the TE_{10} mode in propagation

Although with the classic waveguides is possible to realize slots either on broad and on the narrow sides, with the SIWs only the broad walls are suitable to make the slots. The latter structure is anyway doable and an example of H-plane antenna in SIW technology made by removing some post in the narrow wall is presented in [33].

Beyond the different possibilities to realize a slot over the broad wall of a waveguide, the more pointed are:

1) Place a slot parallel to the longitudinal axis of the waveguide but displaced respect its center;
2) Place a slot parallel to the longitudinal axis of the waveguide over the midpoint, but exited through a metallized post which creates a perturbation of the field inside the guide;
3) Place a slot tilted of a certain angle respect the longitudinal axes of the guide;
4) A combination of the techniques above.

Because of the wide band that the slots have to support and due to fact that the boresight of elementary radiators should fixed over all the frequencies, only the point number 4), which has more degrees of freedom, offer a practicable solution.

In order to enhance the gain of the array, the elementary radiators are placed in a scheme (Figure 4.20), in which they are equidistantly separated in both the direction (X, Y) of the plane. The pitches in X and Y directions are 22mm, correspondent the wavelength in air at the higher frequency considered, this distance avoids the presence of grating lobes. As for the devices described in the previous paragraphs, the structure was simulated as a dielectric filled waveguide, neglecting thus the metallized vias of the SIW. Thanks to the full equivalence between DFW and SIW, in a second moment the vias will be replaced in the narrow wall of the guide.

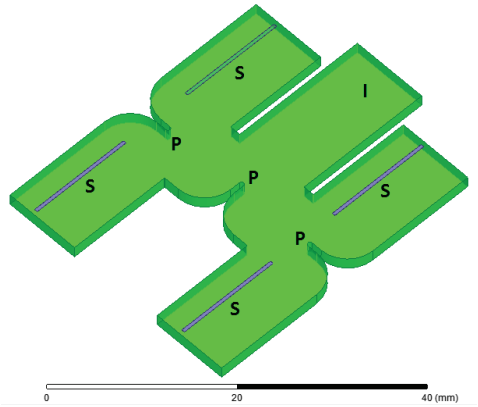


Fig. 4.20: Basic scheme with elementary radiators (2x2) composed by displaced slots where are highlighted with the letters:
I for the input port;
P for the power dividers;
S for the slots

The length of the slots has been chosen in a way [34] to obtain a resonating frequency of 11.75 GHz, the frequency of middle band that is:

$$l_{slot} = \frac{\lambda_0}{\sqrt{2(\varepsilon_r+1)}} \qquad (4.5)$$

Where l_{slot} is the length of the slot that permits a resonance at the wavelength λ_0 (in air) in a substrate with the permittivity of ε_r.

As already pointed out, the configuration with a single slot does not guarantee a fixed boresight of the beam over all the bandwidth, as shown in Figure 4.21.

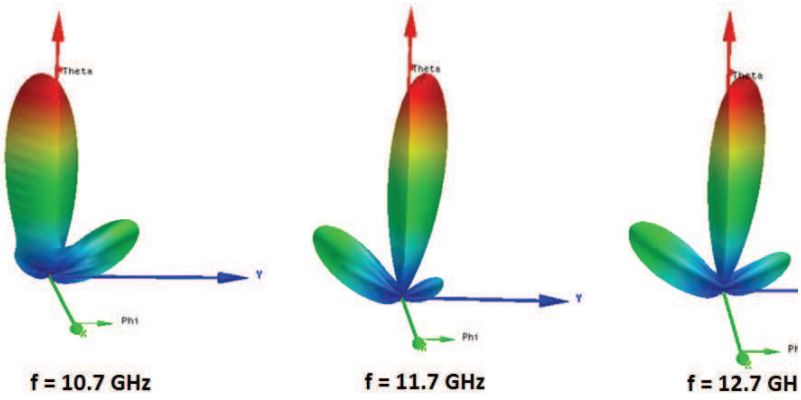


Fig. 4.21: 3D plot of the total gain of the 2x2 elementary radiators with single slot at the lower, middle and higher frequencies of the band

In the paper of Mencarelli et al [35], it is presented a new combination of slots with which is possible to overcome the dependency of the beam on the frequency.
Such a configuration foresee a couple of slots with lengths that are slightly different each other, one placed over the axis of the waveguide and the other slightly displaced that acts as active element. Of course, the slot placed in the center of the guide would not radiate if standalone, then to create asymmetry, an additional metallized via is placed inside the guide. In this way, the distribution of the field is not symmetrical respect the axis of the guide and also the slot placed on it can radiate. Because of their difference of length, the two slots radiate at slightly different frequencies in order to cover better a so wide band.
The initial length of the slots was chosen according to the formula (4.5). Because of the proximity of the two slots, a mutual coupling between them is then established and is not possible to design the slots separately. The system composed by the two paired slots and the via, was simulated trough the simulator HFSS and the related geometric parameters (lengths, distances, positions, etc.) were optimized in order to obtain a fixed beam over all the frequencies of interest. The scheme 2x2 so formed and the boresight of beam at three significant frequencies are shown in Figure 4.22.

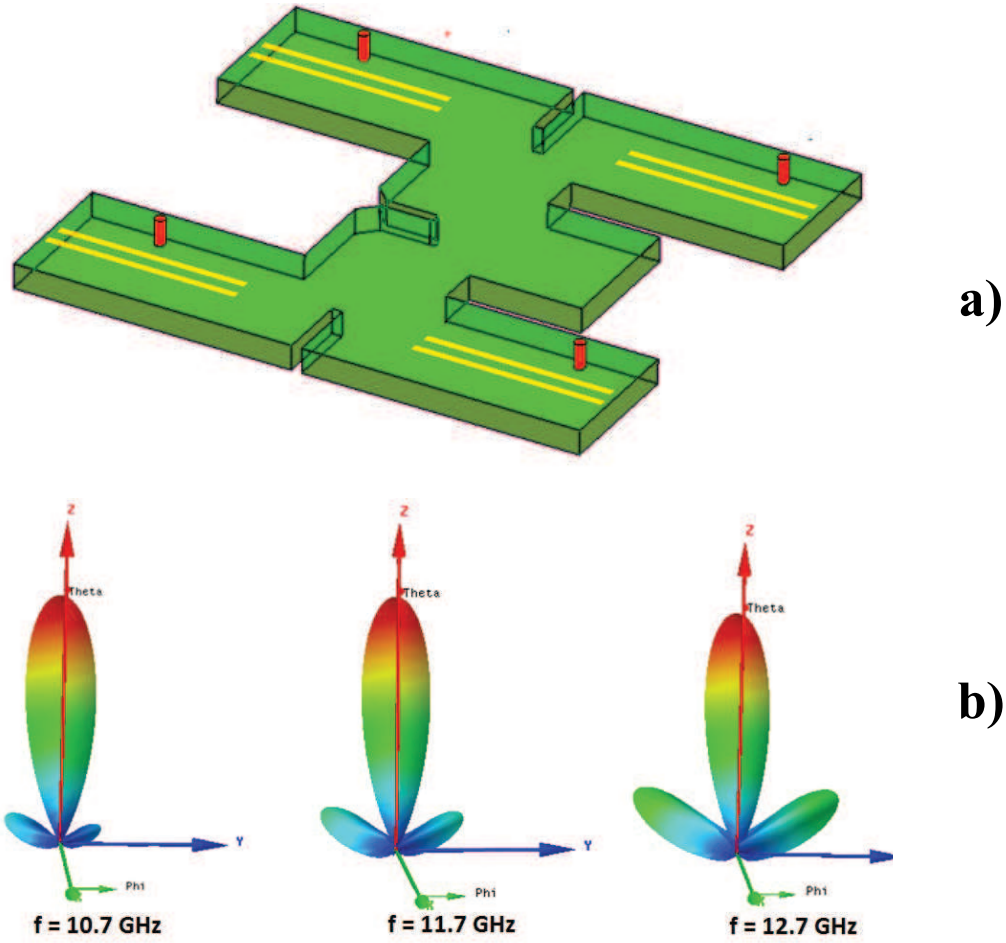


Fig. 4.22: a) Modified basic scheme with elementary radiators composed by the paired slots (in yellow) and the metallized via (in red);
b) Boresight of the modified scheme at the lower, middle and higher frequencies of the band

To validate the new configuration of slots, two stacked sub-arrays, each composed of 2x2 elementary radiators were designed, simulated, manufactured and experimentally characterized.
In Figure 4.23 is shown the top surface of the prototype realized. The substrate is the Taconic RF-35A2 with Dk = 3.5 and Df = 0.0015 with 35µm of copper foil, the process used for the synthetization is described in cfr. 3.

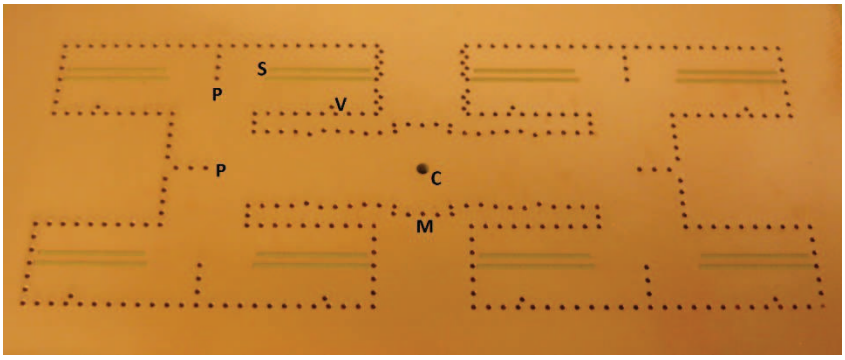


Fig. 4.23: Top view of the first array prototype. Are marked the following relevant parts:
C) hole for the coaxial connector;
M) matching stage for the connector;
P) power dividers;
S) pair of slots;
V) metallized via

The connector SMA has been welded in the middle and the sub-array 2x2 so fabricated was characterized by measuring the reflection coefficient and the radiation pattern.
In Figure 4.24 it is reported the return loss of the sub-array in the band 10.5 – 13 GHz and in Figure 4.25 we can find the simulated and the measured E and H plane radiation patterns at 11 GHz.

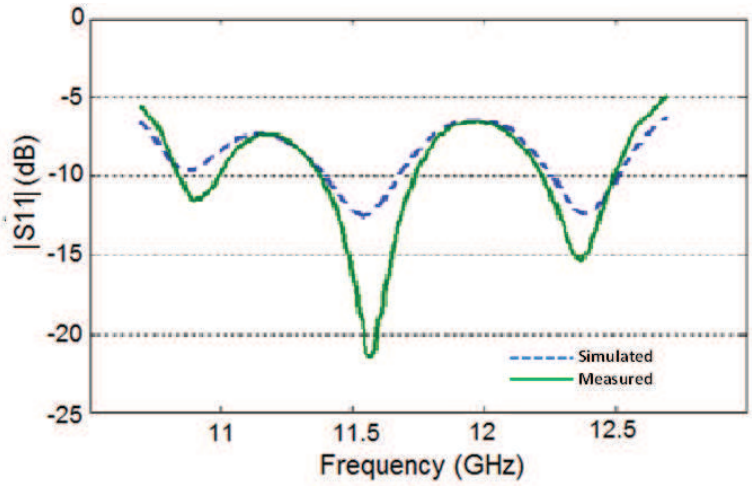


Fig. 4.24: Simulated (blue-dashed) and measured (green-solid) $|S_{11}|$

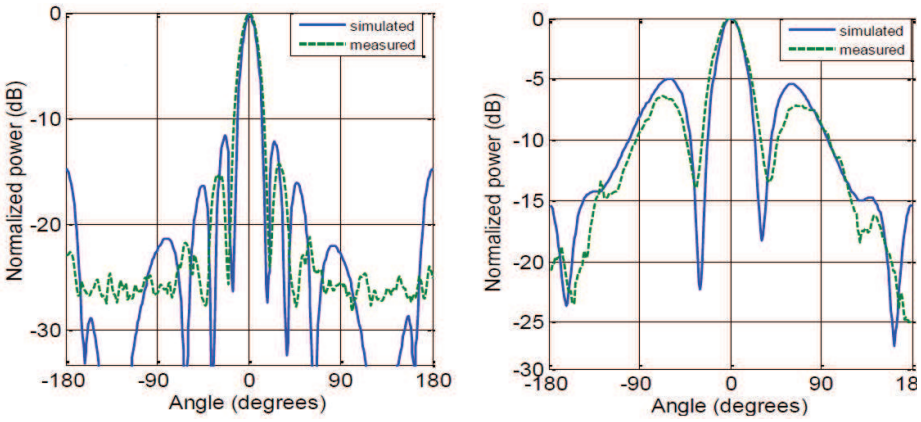


Fig. 4.25: Simulated (blue-dashed) and measured (green-solid) at 11 GHz H-plane radiation pattern (on the left) and E-plane radiation pattern (on the right)

Considering 7 dB of return loss, the bandwidth is wide (20%) and covers the range of interest 10.7 – 12.7 GHz. Unfortunately, the matching is not so high because of the limitations due to the optimization on the beam. It was chosen to sacrifice the matching to keep the beam as more close as possible to the boresight direction that is orthogonal to the plane containing the antenna ($\theta=0°$). In any case the matching of 7dB, correspondent to the 80% of the through power, is sufficient to receive the DVB-S signal.
The measured radiation patterns agree with the simulations, at less than 2 dB attributable to deviation on the dissipation factor (cfr. 2.2) and fabrication tolerances. On the E-plane it can be noticed a level of the secondary lobes that is about 13.5 dB less respect the maximum and it is in agreement with the uniform distribution. In both planes E/H, the beam is centered at $\theta=0°$ according to the project specifications.

4.5.2. Feed line

The feed line for this type of application was chosen in terms of efficiency, compactness and cost. In Chapter 2, were discussed all the relevant properties of the dielectric materials were discussed in order to find the more suitable ones for this purpose. Based on the cost and on the performances of the dielectrics, two significant materials emerged: the Taconic RF35-A2 (Dk = 3.5, Df = 0.0015) and the Rogers Duroid 5880 (Dk = 2.2, Df = 0.0009).
To obtain a planar and uniform array, that guarantees the maximum gain compared to the area of the array, the feed line should equally split the power at each radiator and the distances from the input port to each radiator should be identical.
One common feed method, widely used in the microstrip technology, is known as "corporate" scheme (Figure 4.26). The corporate feed line has a single input port and multiple feed lines in parallel constituting the output ports; each of them is terminated in an individual radiating element. The fundamental configuration of a corporate feed consists of a branching network of two-way power dividers and segments of lines.

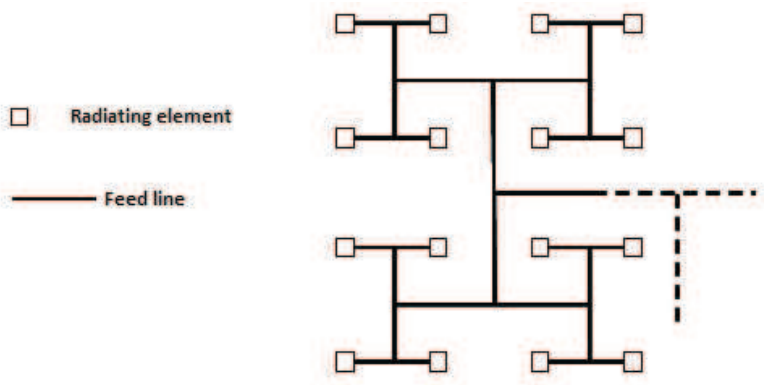


Fig. 4.26: Sketch of the corporate feed network

Because of the H-shape of the elementary radiators (cfr. 4.5.1), only a limited space (around 8 mm) between two adjacent "H" is available to insert a segment of line and then to realize the corporate scheme; the minimum dielectric constant that permits to obtain a segment of guides overcut, filling the abovementioned space is 3.5. The latter binding forces the choice to the Taconic RF35-A2, which although with a higher dissipation factor, allows hosting both the radiators and the feed line on the same substrate. The use of the Duroid 5880 was discarded for following reasons: 1) the cost per square area is roughly 2.5 times higher respect the Taconic; 2) an additive layer would be necessary to feed the radiators; 3) the complexity of the process, and thus the cost, increases for a multilayer board.
All the radiators, having an identical distance from the main feed point, benefit of a common electrical path, which guarantees a boresight of the beam independent of the frequency.

The disadvantage for this kind of structure is that it requires a long transmission line between the radiating elements and the input port. In presence of lossy materials, it is not convenient to increase the size of the antenna over a certain value because of two opposite effects: the gain of the antenna linearly grows respect its area, whereas, the losses of the feed line attenuates exponentially respect its length. Moreover, as the size of the antenna increases, also the number of components constituting the feed line increases, so an additive attenuation factor due to mismatching losses has to be taken into account.
In order to place the radiating elements and the feed network on the same substrate, the use of power dividers with three ports is obliged, although they suffer from a modest matching if compared with the directional couplers, they are compact and can be placed between the radiators.

The constitutive elements of the feed network are:

1) An SMA to SIW transition;
2) Segments of waveguide;
3) Three ports power dividers, with different matching stages.

Unlikely the components presented in the previous paragraphs (cfr. 4.1.2, 4.2, 4.3), here the blocks have been designed in order to maximize the matching of the entire feed line.
Considering that the computational load grows exponentially when simulating a series of elements, a corporate feed line network composed of many components combined would be impossible to simulate efficiently. In order to keep contained the simulation time, all the blocks constituting the antenna have been simulated separately and the frequency response of the whole beamforming network was retrieved as composition of Y matrix of the single elements.
In Figure 4.27 is shown the frequency response of the first block, that is a modified version of the device described in 4.1.2. Here, the return loss at the port 1 (the coaxial connector) is improved at the expense of the ports 2 and 3.

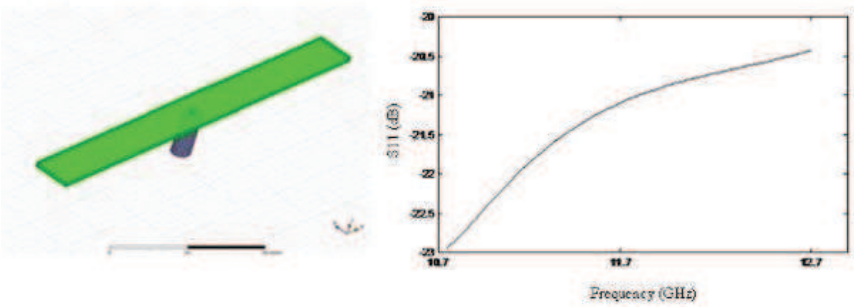


Fig. 4.27: Three port power divider on the left and the relative frequency response on the right

The reflection coefficient at the coaxial port is better of -20dB over the band of interest (10.7-12.7 GHz).

The second element constituting the feed line is an H-plane three-way power divider. In Figure 4.28 we can find the first two blocks and the frequency response of their composition. The reflection coefficient seen at the coaxial port is better of -15 dB over the entire band. It is well noticeable the effect of the constructive and destructive interferences, that inevitably come out in presence of a wide band and sizes of many wavelengths. The matching is reduced of 5 dB compared to the single coaxial transition.

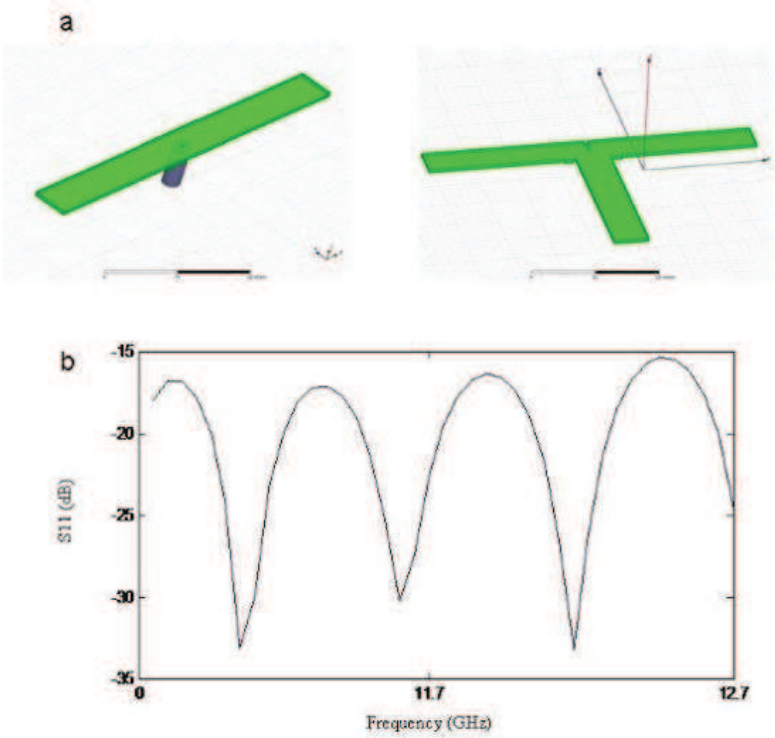


Fig. 4.28: (a) The first two blocks of the feed line: the coaxial transition and a power divider. (b) Reflection coefficient of the composition of the first two blocks seen at the coaxial port

Because it is not foregone that the best matching of a series of two or more blocks is obtained by maximizing the response of each of them, an additional tuning stage, formed by a stub, is placed in proximity of the septum in the H-plane power divider. The size and the position of the stub are obtained through parametric simulations in order to maximize the return loss of the composition of the blocks.

With the same methodology, other blocks are added to the feed line with the intention of distributing the signal as uniformly as possible. Other power dividers and segments of waveguide with sizes optimized with the intent to maximize the return loss at the coaxial port, realize the feed network for the elementary radiators (Figure 4.29).

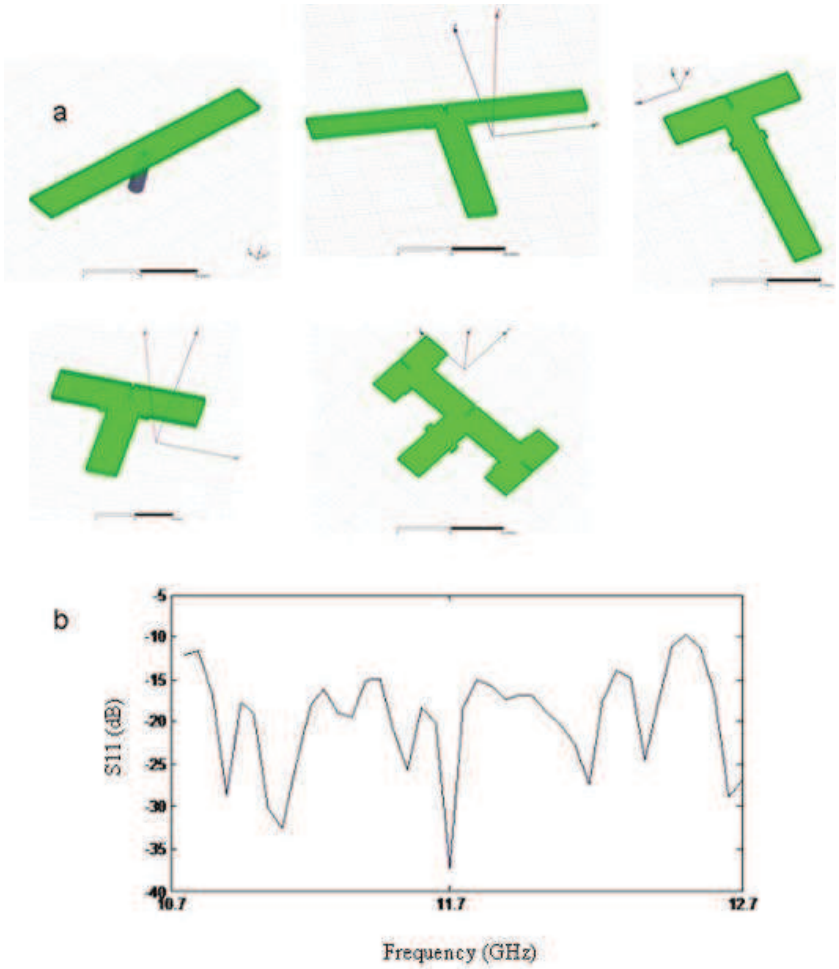


Fig. 4.29: (a) Five relevant blocks constituting the feed line. (b) Overall reflection coefficient of the composition

The abovementioned blocks permit a division of the signal in 64 ways. The return loss of the entire structure, calculated at the coaxial port, is better than 10 dB over the band considered. It is quite clear that the matching worsens as the number of components increases. This effect, however, is slightly mitigated (Figure 4.30a) from the losses of the material that constitutes the devices. In fact, the lossy nature of the materials lead to attenuate the signal passing through them, on the other hand, it attenuate also the reflections due to the mismatching of the blocks, improving then the overall coupling.

Although the losses represent a positive outcome under a point of view of the matching, these lead a drop of the useful power, in fact, part of the power is dissipated along the device for the Joule effect.
For a lossless 64-ports device, the theoretical transmission coefficient at each port is -18 dB. Figure 4.30b shows a comparison between two simulations of the BFN, here designed, in the ideal case (Df = 0) and in the real case (Df = 0.0015). It can be noticed a difference of about 2 dB that represent the power loss of the signal.

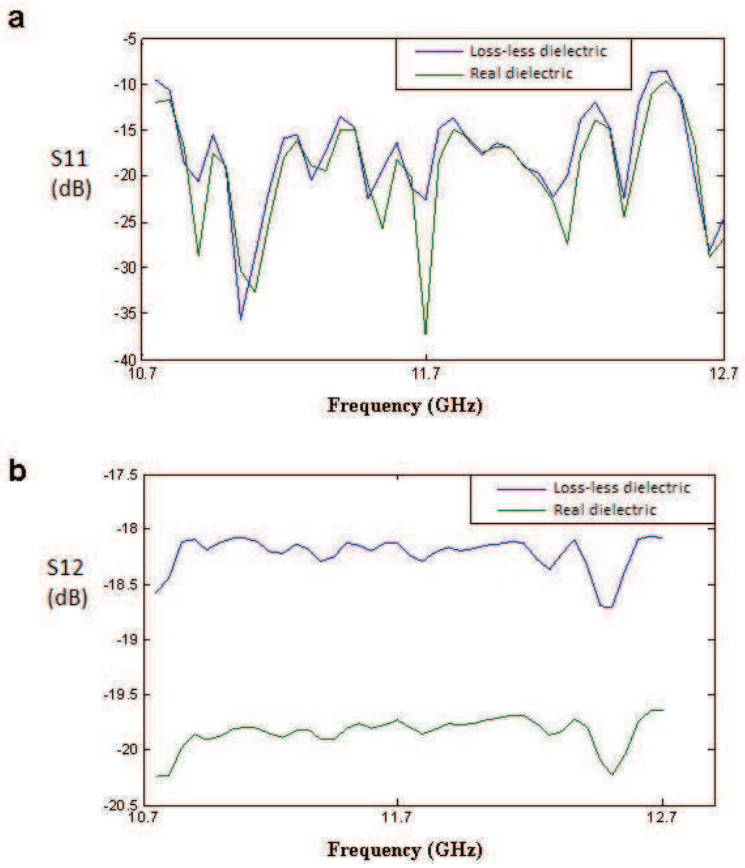


Fig. 4.30: Comparison between simulated S11 (a) and S12 (b) of the BFN. In green the real dielectric with Df = 0 and in blue the ideal dielectric with Df = 0

4.5.3. Radiating blocks and external region

Generally speaking, the simulation of small prototypes, in terms of wavelength, is computationally doable with commercial solvers running on any standard workstation. Whereas, when the dimensions of the components grow, the simulation times become so long that it is impossible to optimize the devices in a reasonable time span.
In this specific case, considering the dimensions of the sheets of laminate commercially available and the 3 dB power dividers designed, the maximum number of replicas of elementary radiators (cfr. 4.5.1) that can be used to compose the planar array is 8x8, corresponding to a number of slot of 32x16 and an area of 352x352 mm^2. Furthermore, being an antenna, shall be considered also a radiating box over the slots sufficiently wide to emulate the condition of free space propagation.
In order to simulate efficiently the structure and optimize the geometry (shape, length, separation) of the slots a different approach is used, based on both simulation results and analytical method where the inter-element coupling was taken in account.
In this way, the whole planar array is divided in two regions, and one of each is analysed separately. The synthesis method used as reference comes from the paper of Morini et Al. [36]. Here it is called "internal region" the feed network constituted from the segments of line and the power dividers, dually, the "external region" is represented from the slots and the radiating space. The two regions are interconnected through waveguide having the same cross-section of the slots and a length that is equal to the thickness of the copper where the slots are etched.

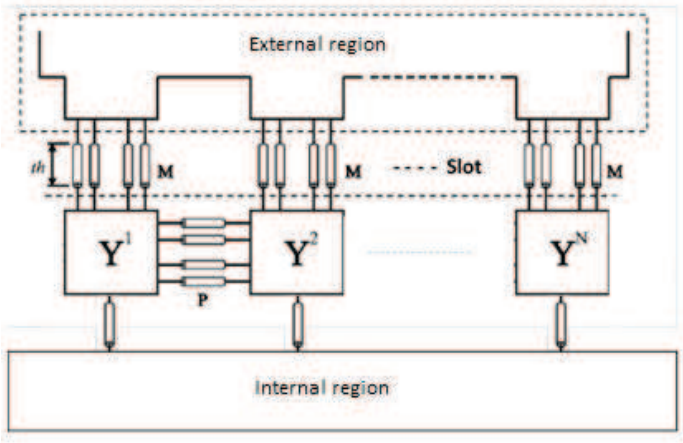


Fig. 4.31: Composition of the internal and external region through the blocks containing the slots, represented by the admittance matrixes; *th* is the thickness of the copper where are etched the slots and M is the number of the accessible modes per slot

The situation described is analogous to the scheme in Figure 4.31: a certain number of circuital blocks, characterized by their admittance matrixes (Y^1 … Y^N) are connected internally from the structure composed of power dividers and segments of line, whereas, externally they are connected by a unique block through the M accessible modes for the slots by the number of slot for each radiating sub-array.
The blocks constituting the internal region have been developed (cfr. 4.1, 4.2, 4.3) to obtain the best return loss in 2 GHz of bandwidth (10.7 – 12.7 GHz). Conversely, the geometry of the slots has to consider not only the matching with the feed network but also the bond of the couple that ensures a fixed boresight at all the frequencies.
In the external region, all the iterations between slots are calculated in a semi-analytic way. Practically, the mutual coupling between slots became negligible when their distance is greater than some wavelengths. This simplification permits to ignore many contributes, therefore reducing the simulation times. Others simplifying assumptions are made: i) only one accessible mode (M = 1) for each slot, thanks to the strong constraining of the SIW technology, ii) infinite metallic plane containing the slots in the external region, iii) Dielectric-filled rectangular waveguide approximation of the SIWs.

4.5.4. Experimental characterization

The method described in cfr. 4.5.3 allows to synthesize efficiently a wide planar array, optimizing many parameters such as the length of the slots and their arrangement over the plane. The definition of the latter parameters leads the design of the array in Figure 4.32.

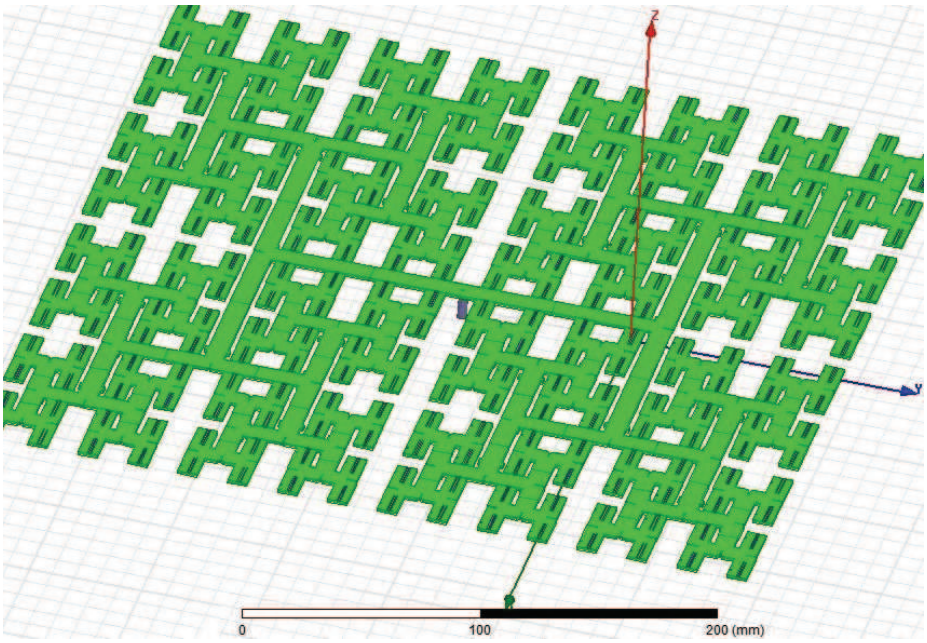


Fig. 4.32: CAM representation of the composition of feed line and the elementary radiators. In the middle of the structure is placed the coaxial transition

As can be seen in the previous image, the BNF is designed over a single dielectric layer and the same layer contains the elementary radiators. The prototype foresees 16X16 radiating elements, each constituted of a couple of radiating slots.

Thanks to the equivalence waveguides – SIW make it possible to realize such array with the process described in Chapter 3, with the only shrewdness to resize the width of the SIW components according to the pitch and the diameter of the vias with which they are realized. The first prototype realized is shown in Figure 4.33.

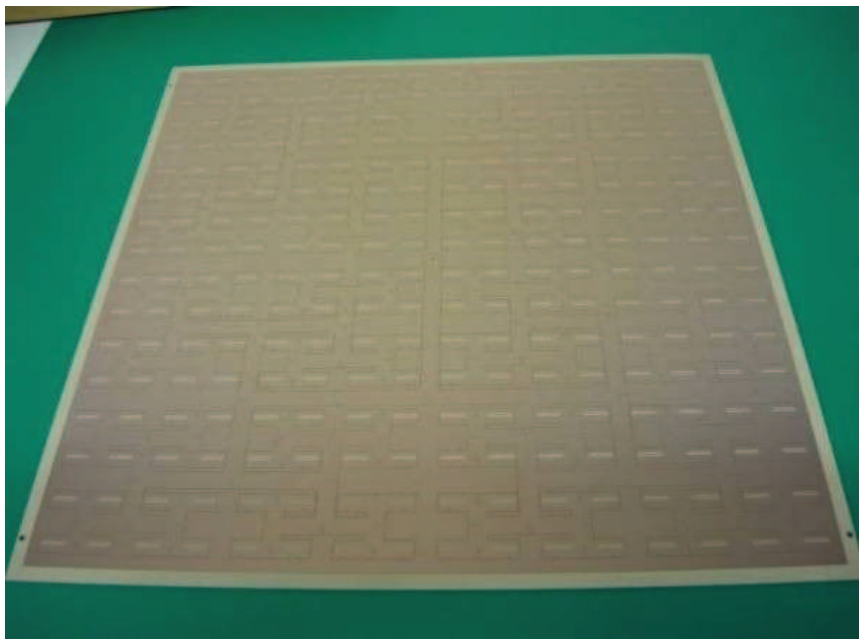


Fig. 4.33: First prototype of the SIW antenna, with dimensions of 352x352 mm, realized over a substrate of Taconic RF-35A2

4.5.4.1. Return loss

The reflection coefficient of the antenna, measured at the coaxial port is reported in Figure 4.34.

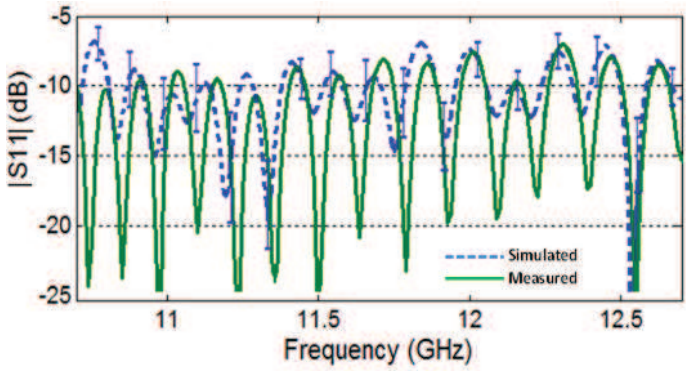


Fig. 4.34: Reflection coefficient in the band 10.7 – 12.7 GHz. Simulation (blue dashed) and measurement (green solid). The blue marker defines the rage of variability of tanδ

The oscillating characteristic of the frequency response is mainly due to the dimensions of the BFN, containing components length many wavelengths. The band limitations of the power divider and radiating elements, together with the length of the lines of waveguides is the origin of such a non-uniform response.
The matching at the input port is better than 7 dB that is not so high, but it is the best trade-off obtained on a band wide 2 GHz. Keeping in mind that the simulations have been performed with dielectric parameters retrieved from measurements (Cfr. 2.2) instead of those declared from the substrate supplier, the abovementioned graph shows a very good agreement between the simulations and the measurements, in spite of the fabrication tolerances and the manual welding of the SMA connector that is an unpredictable factor.
In the graph, the blue curve is calculated with tanδ = 0.0030 and the markers define its possible range of variability, in this case [0.0030±0.0008].

4.5.4.2. Radiation pattern

The radiation pattern of the antenna has been measured beside the Laboratory of Electromagnetic Fields and Telecommunication, University of Taranto, which is equipped with a near field measurement system "Starlab". The near field system estimates the radiation characteristics (for definition in the far field), from measures of energy in the near field region. The measured radiation pattern being is shown in Figure 4.35.

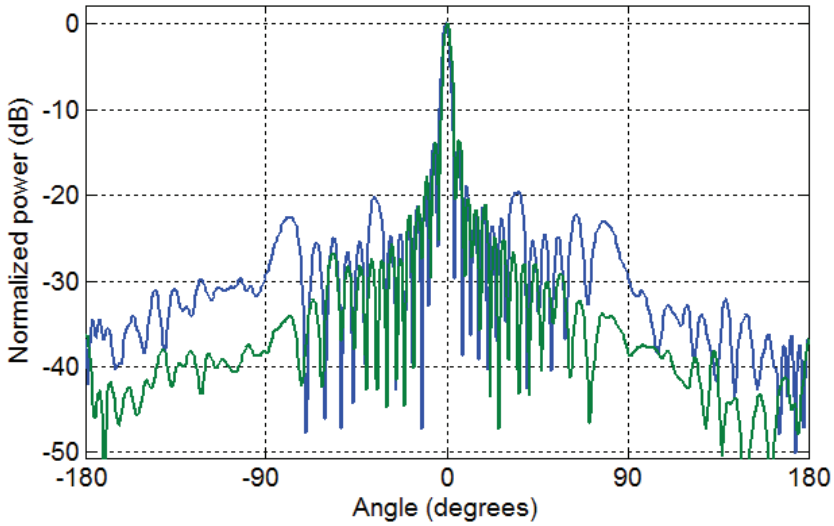


Fig. 4.35: Radiation pattern in the E-plane (blue solid) and in the H-plane (green solid) of the planar array at the frequency of mid-band 11.7 GHz

This measure is related to the frequency of mid-band 11.7 GHz. As expected, the pattern is in accordance with the uniform distribution, symmetric respect the boresight direction and with lateral side lobes at about -13.5 dB. The graph shows also an improved directionality in the H-plane compared to the E-plane, due to the directionality of the elementary radiators. The slots, in fact, have a wider extension in the H-plane that confers a higher gain.
Particularly interesting it is the analysis of the shift of the main lobe with the change in frequency inside the band of interest 10.7 – 12.7 GHz. The Figure 4.36 shows the displacement of the main lobe for different frequencies, which is contained in 0.15°. In the H-plane, the displacement of the main lobe is negligible (Figure 4.37).

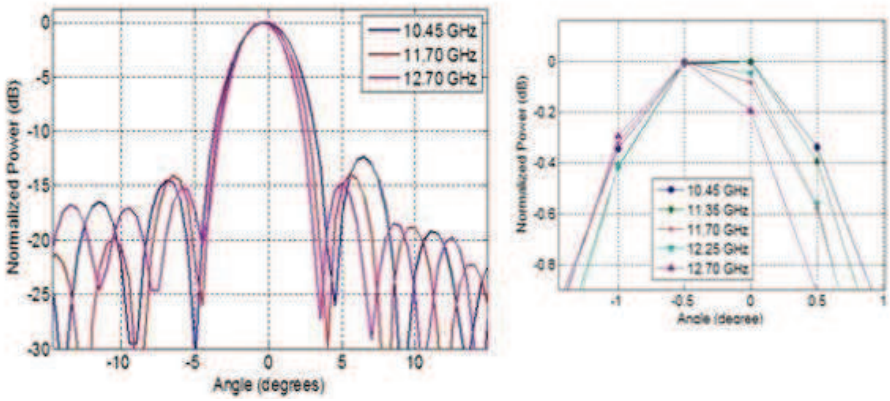


Fig. 4.36: Shift of the main lobe in the E-plane measured at the middle and peripheral frequencies

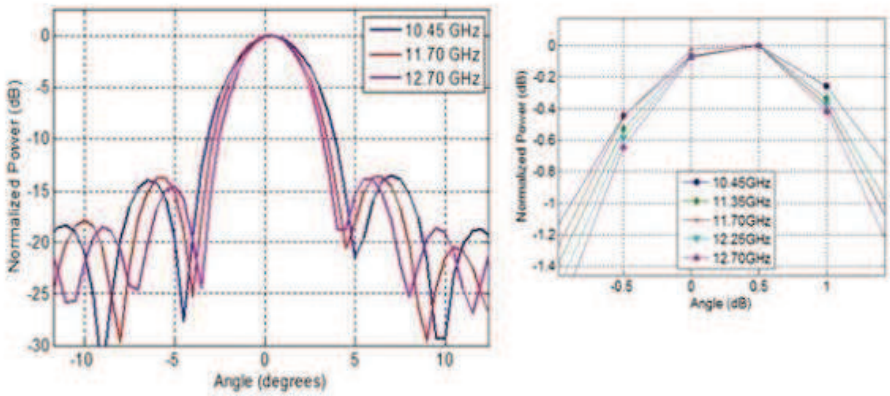


Fig. 4.37: Shift of the main lobe in the H-plane measured at the middle and peripheral frequencies

4.5.4.3. Gain

Finally, it is reported in Figure 4.38 the comparison between the gain which has been calculated in a semi-analytically way (cfr. 4.5.3) and the gain which has been measured through the near field system Starlab.

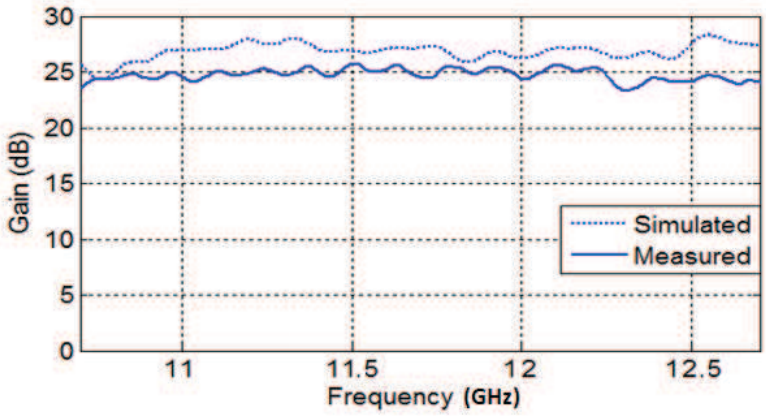


Fig. 4.38: Simulated (solid line) and measured (dashed line) gain vs frequency

The differences between the simulation and the measures are around 2 dB that can be attributable to an underestimation of the losses in the dielectric and in the copper.

Chapter 5.

Fabrication process for losses reduction

Most of the researches published on SIW components exalt their merits in terms of compactness, low loss and easiness of fabrication, but the size of the components has to be taken into account. It is clear that the losses of a small component influence only in a limited part its performances. As the dimensions of the components grow, as per of an antenna with high gain, the losses become more and more significant and to keep them contained often low loss materials are used. In Chapter 3 it is shown the fabrication process of SIW components realized with a low loss substrate that is not banal. Also many additional steps compared to standard laminates (FR4) are needed to grant the specification requirements. Another drawback of the use of low loss laminates is their cost, which is in contrast with the purpose of the Project that is the replacement of traditional metallic TV dishes, available for few dollars.
Moreover, in literature, a great part of the works on the SIWs realized with PCB technology, is at frequencies below the mm-wave band because of the dielectrics inherent lossy nature. At frequencies beyond the 30 GHz, IC technology (for instance TCC – Temperature Cofired Ceramic) is preferred but the used high Dk substrates used make the SIWs so small neglecting the realization of tolerances.
The ultimate transmission medium that minimize the propagation losses and can be efficiently used either for microwaves, millimeter waves and above is the traditional metallic hollow waveguide. On the other hand, waveguides are bulky, heavy and their high cost is due mainly to the metallurgic fabrication process.
The intent of the SIWs, as originally intended [37], was to reproduce the waveguides in a planar form, keeping their advantages but the problems derived from used materials emerged soon.
What makes the SIWs original is the trick of the metallized vias along the guide that imitate the solid lateral side of a metallic waveguide and permit the propagation of the fundamental mode. Obviously, the rows of vias, if compared with the continue side wall of a waveguide are less performing under the losses point of view. The incomplete shielding led a localized (not distributed as for the waveguide) density of current on the vias with a subsequent ohmic loss due to their finite conductibility and a radiation loss due to the formation of leaky waves through them. However, these two losses can be kept confined with opportune design rules [38].
Dielectric loss is the main source of loss in SIWs and it is significantly higher compared the other two mechanisms, and the only way to reduce it is acting on the filling material. In the following chapter it is presented a novel manufacturing process for the fabrication of a SIW with quasi-zero dielectric loss. The key idea is to remove the dielectric material from the internal part of the SIW and to enforce the field to travel into the air that has a very close to zero loss-tangent value.

5.1. Planar hollow waveguide: the state of art

The idea of the dielectric removal from a SIW is not new. In 2014 two papers treat this topic with different approaches. In the paper of Mohammadi [39] it is presented a transmission medium called "Partially filled SIW (PSIW)", where the middle part of the guide is constituted of air and dielectric while the top and bottom walls are realized with metal plates, stacked and connected with screws. In detail, the middle part is machined to remove the dielectric inside the guide (Figure 5.1), except for two small areas along the guide that will host the metallized vias and permit the confinement of the travelling field.

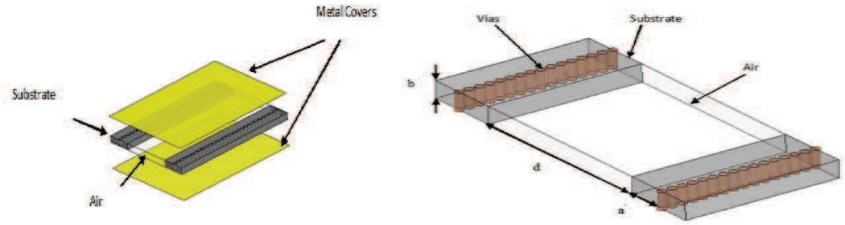


Fig. 5.1: Concept design of a PSIW on the left and detail of middle part of the PSIW on the right. The grey part are the dielectric hosting the metallized vias, the yellow parts are the top and bottom covers (Courtesy of [40])

The main criticism of the structure is represented on the screws used to join the covers and dielectric part inasmuch:

1) the presence of a metallic screw in the proximity of a not perfectly self-shielding structure could affect its frequency response;
2) the alignment of the layers has to be very accurate to avoid deviation from the simulations, it could be improved with the use of pins;
3) screws allow the application of a constant pressure only in the immediate neighbourhood of it, the area at constant pressure is limited as less rigid is the material. Moreover, because teflonic materials are soft, they suffer of deformations introduced by the screws.
4) an additional radiation loss could be encountered if there are points of poor contact between the layers.

Part of the problems abovementioned can be contained if the number of the screws increases, but in this way the weigh and the volume of the final circuit increase, nullifying the advantages of lightness and compactness of the SIWs.
Components manufactured in this technology (Figure 5.2) are bulky, heavy and they are not suitable for the mass production.

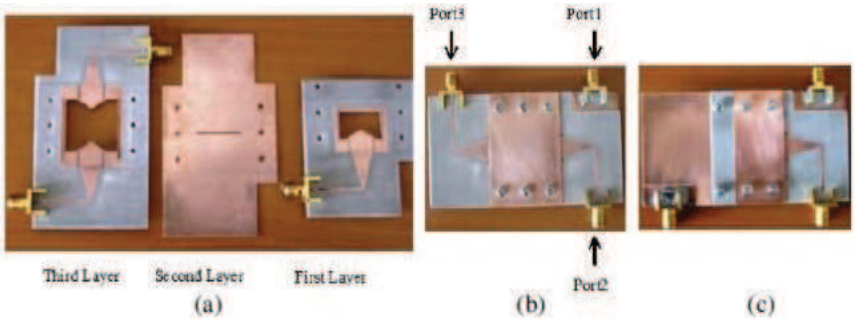


Fig. 5.2: Example of a 3-port directional coupler in PSIW. (a) Three layers of PSIW without the top and bottom covers, (b) top and (c) bottom view of the components so realized. (Courtesy of [40])

Another paper in which it is proposed an alternative structure called "Hollow substrate integrated structure (HSIW)" is from Jin [41]. Here, an equivalent hollow structure is realized through a progressive-lamination LTCC (low temperature co-fired ceramic) without the use of screws as happened above. A sketch of the mentioned structure is presented in Figure 5.3.

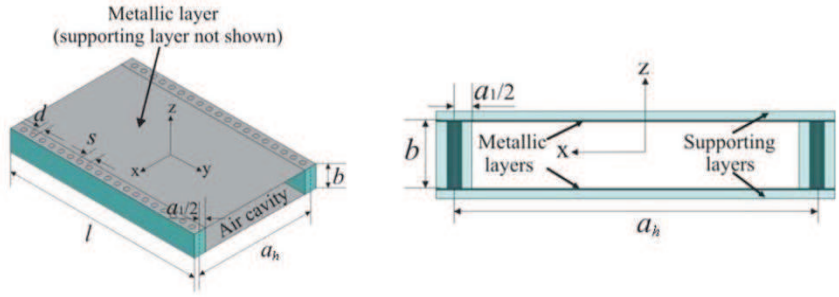


Fig. 5.3: 3D view on the left and cross-section view on the right of a HSIW. (Courtesy of [41])

First, a series of sheet of LTCC tape are stacked and pre-laminated to provide sufficient densification and for the material stabilization. In this stage only the sheets constituting the main body take part, while the external layers are processed separately.
Once the middle part is formed, a rectangular slot (will become the air gap) and the vias are cut out with a laser-drilling machine. A conductive paste is plugged inside the vias and over the covers, here a thin layer, to form the narrow and the wide sides of the guides respectively. Even in this case the three blocks constituting the guide are aligned and laminated using a

uniaxial laminator. Finally, according to the LTCC manufacturing process, the stack is co-fired for around 36 hours. In Figure 5.4 it is reported the main body of the half-processed guide and the HSIW so formed.

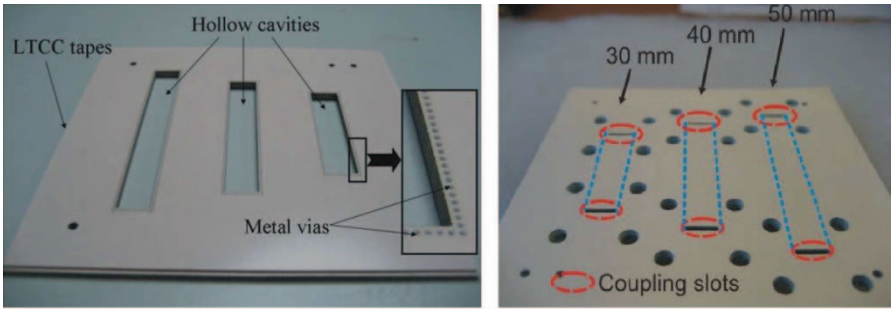


Fig. 5.4: Half-processed HSIW with the detail of the vias plugging on the left and the structure at the final stage on the right. (Courtesy of [41])

Unlike the configuration proposed from Mohammadi [39], the HSIW does not foresee the use of the screws for the connection of the body but a more stable and repeatable method as the press lamination. The LTCC process confers to the structure hardness, solidity and above a stable electrical continuity between the covers and the plugged vias.
The weak point of this process is the silver paste used and the method with which is applied:

1) the silver paste used in this process is the Dupont LL601, which has a resistivity 3 times higher respect the copper (ρ_{LL601} = 5 mΩ/sq vs ρ_{cu} = 1.68 mΩ/sq, both normalized to a sheet of 10μm). In this way the dielectric losses decrease, but at the same time the losses in the metal increase.
2) the application of the paste through a screen printing machine is limitative. For instance is not possible to cover vertical edges such as the internal part of the slots that permit the coupling. Across them, a part of the EM energy will be lost, increasing in this way the radiation losses.

Furthermore, LTCC technology is more costly that for PCBs, and the times of realization are longer.

5.2. Dielectricless SIW

Although the two configurations presented in cfr. 5.1 exhibit a reduction of the total losses; these introduce drawbacks already pointed out. Besides, in both cases, the processes have been designed for the fabrication of prototypes and they are not suitable for the mass production.
In the following paragraphs it is presented a novel structure, here called Dielectricless SIW [42], based on the processes used in the PCB industry. The idea is the same of [39] and [41]: removing the dielectric substrate inside a SIW will reduce the dielectric losses, but it has been thought in the optic of costs reduction, process automation and hence orientated for the series production. Moreover, the structure so realized is fully self-shielding (for the TE_{10} mode) and conserves the qualities of a planar technology, namely, low profile, lightness, easy integration of passive and active devices and manufacturing repeatability.

5.2.1. Fabrication methodology

The waveguide is derived directly from a laminate of dielectric material, typically FR4, which is robust, well workable, and low cost. The laminate consists of two copper foils interspersed with a prepreg layer that has already reached the glass transition temperature, acquiring in this way characteristics of rigidity and inalterability with respect to temperature. The main body of the waveguide profile is obtained through a Z-controlled milling machine. Milling is the machining process of using rotary cutters to remove material, dielectric and copper, in a direction with the axis of the tool. Computer numerical control (CNC) milling machines are used frequently to realize pits, buttonholes and slots over the PCBs. Here the milling cutter was used to create a uniform notch over the laminate. The in-plane dimensions of the groove have to take into account for the subsequent metalization and thus the shrinkage of the useful width (Figure 5.5). Yet, the laminate thickness has to be selected in order to ensure the mechanical stability of the final circuit for the desired depth of the groove. Here, the laminate machined is 2 mm thick with the pit depth of 1.5 mm. The example in Figure 5.5 makes visible also the holes for coaxial connectors, which can be realized in this phase.
After the milling phase, the exposed dielectric is treated in a chemical bath in order to facilitate the ion acceptance. Next, a layer of copper is grown using standard PCB processes, such as chemical deposition or electroplating, depending on the thickness of the copper layer required, which can vary from few microns to tens of microns (Figure 5.6).

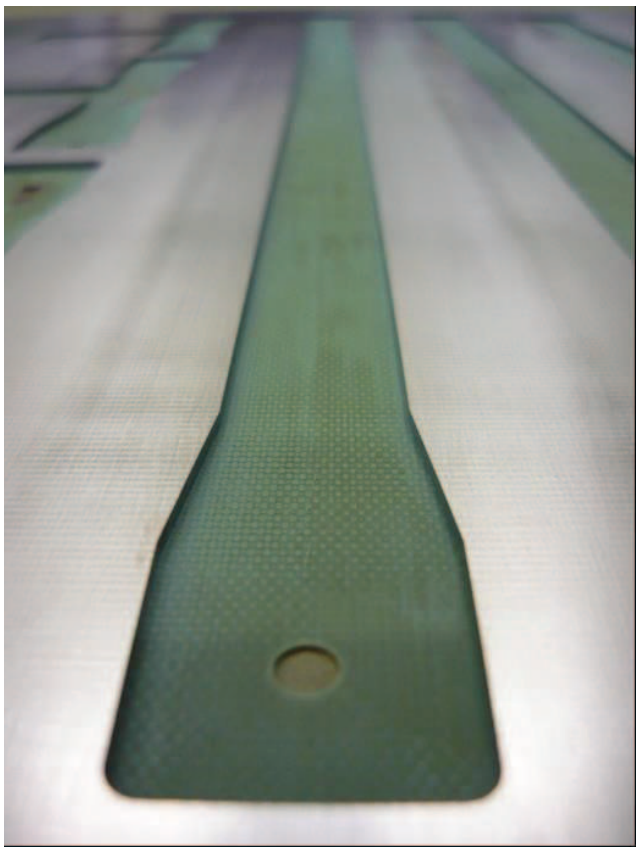


Fig. 5.5: Milled base material laminate. In foreground, the transition for the SMA connector

Of course, the minimum copper thickness to be deposited has to exceed the skin depth at the working frequency, making the guide self-shielding. Higher thicknesses of copper are employed in order to reduce metal losses.
Another laminate of lower thickness (0.25 mm in this case) is then used as cover, forming the top face of the waveguide. This substrate is also machined in order to host the necessary holes for coaxial connectors.
Once the two parts have been metallized with a copper deposition of about 36 μm, it is necessary to bond them together to obtain a single body. Although there are on the market conductive adhesives, these have many drawbacks. In particular, their conductivity is generally very low as compared to copper, and, in addition, they do not guarantee the same adhesion capacity as polymerized prepreg, that is fiber weave impregnated with resin bonding agent.

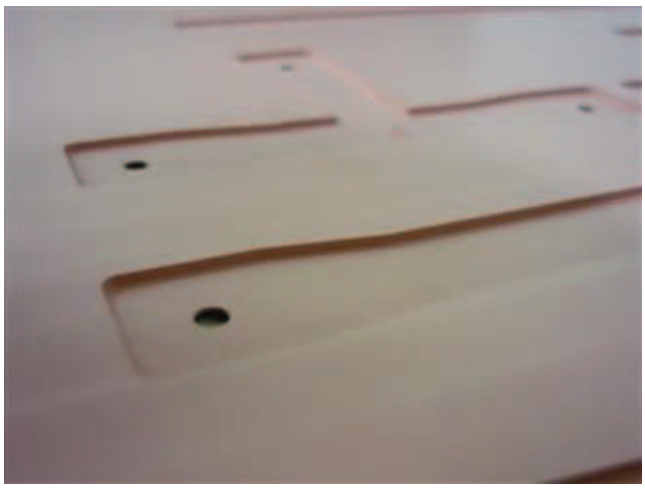


Fig. 5.6: Panel after the metalization process. It appears completely covered with copper

For these reasons, the two parts of the guide are glued through a thin layer of prepreg that, although not conductive, binds them strongly and confers to the guide greater mechanical stability over time. Prepreg is previously worked in such a way to leave uncovered the milled zones (Figure 5.7).
The aperture on the prepreg has to be increased, in order to account for the enlargement it will suffer during the next lamination process to fill the gap between the two parts of the guide and, at the same time, to avoid an exceeding flowing inside the guide. Therefore, the best candidate is a family of prepreg named "no-flow" allowing an excellent control of resin expansion. The use of this kind of prepreg is obliged because its resin flow control, in fact the expansion of the prepreg and the thickness after the press cycle can be predicted, as it is a well-known phenomenon. Anyway, the use of fluid conductive adhesives, such us solder paste or silver-based glues, was also considered, but was discarded because of the impossibility to predict their distribution after the bonding. As a matter of fact, there is a real risk of partial filling of the hollow with consequent worsening of the repeatability of the fabrication process.
Prepreg used is Tuc TU-84P NF, with a thickness of 60 μm after the press cycle. In the prototype proposed, the oversizing of the aperture on the prepreg was chosen equal to 20 μm. This value is preliminary estimation of the resin flow expansion.

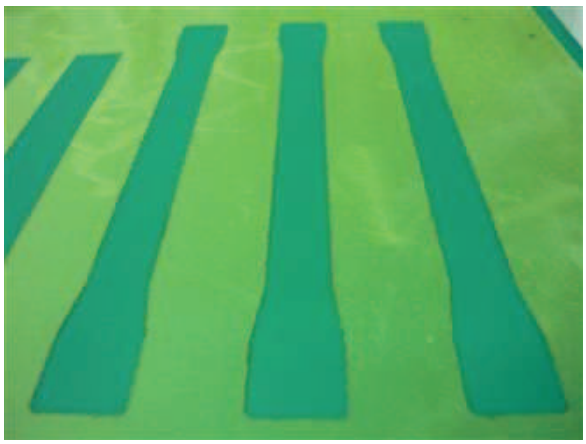


Fig. 5.7: Laser scoring of sheet of no-flow prepreg

The two parts constituting the guide, together with the prepreg, are aligned using pins. The same apertures carried out on the prepreg, are realized on some sheets of Kraft paper (Figure 5.8). Generally, this particular paper is used to ensure uniformity of pressure during the lamination of multilayer PCBs. In this case, the apertures are required to press only over the parts of the panel complementary to the pit, in order to avoid deformation of the guide geometry during the press stage. The two parts constituting the guide, the prepreg and three sheets of paper for a thickness of 3mm in each side are aligned using pins, and the mass-lam formed (Figure 5.9) is then laminated.

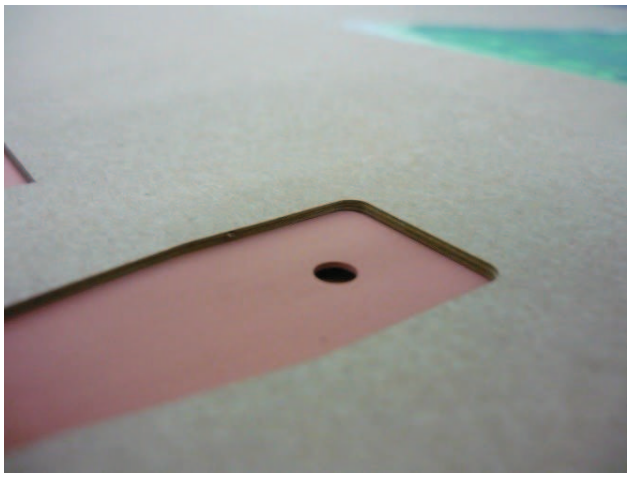


Fig. 5.8: Top view of the mass-lam. Three scored sheets of Kraft paper ensure the perfect rectangular geometry of the guide

At this stage, combined mechanical and thermal actions allow the resin in the prepreg to liquefy, thus bonding the two halves. The resin, expanding, compensates the enlargement of the aperture on the prepreg and forms the narrow side of the guide.
Electrical continuity between superior and inferior laminate is guaranteed through two rows of conductive vias along the guide (Figure 5.10). This method of containment of the EM field is analogous to that used for SIWs

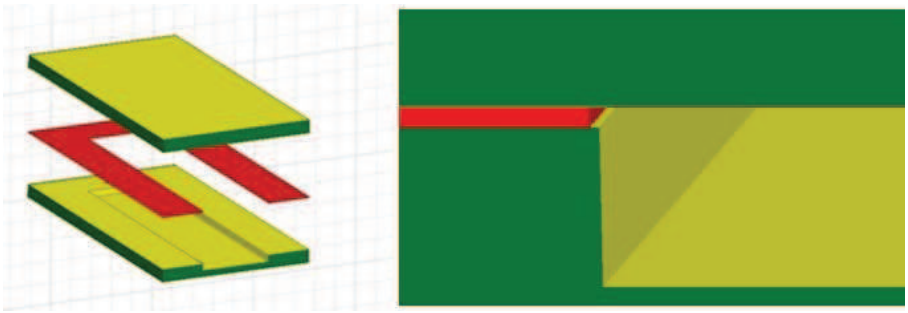


Fig. 5.9: Resulting mass lamination composed by the milled guide (yellow part on the bottom), the prepreg (red sheet) and the cover (yellow part on the top). On the right, the detail of the oversizing of the aperture over the prepreg before the lamination process. Thickness not in scale

The distance and the diameter of the metallized holes have been chosen according to the condition to minimize the radiation losses in SIW technology that is $s/d = 2$ [43]. In this case the diameter is set equal to 500 μm and the spacing between holes equal to 1 mm. Simulations show that the distance between the center of the metalized holes and the edge of the pit has low influence on the propagation constant; hence it has been arbitrarily chosen equal to 1 mm. Copper deposition inside the holes is 30 μm, which is much greater than the skin depth in the conductor at the frequencies of interest.

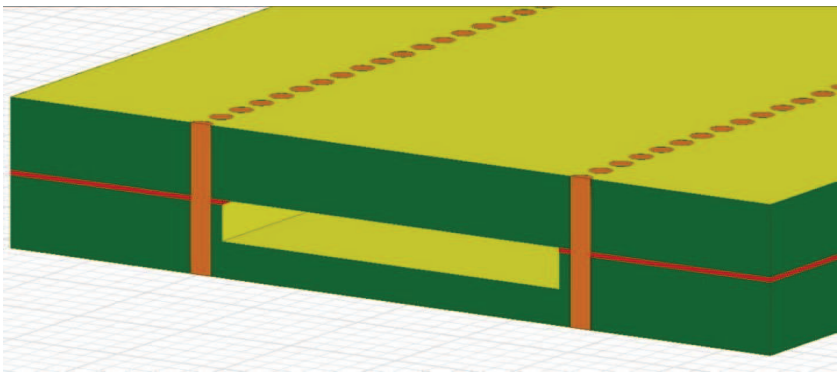


Fig. 5.10: Sketch of the section of the waveguide. The green part is the dielectric, the red part is the prepreg and the yellow parts are the metallized faces. Electrical continuity is enforced by vias (orange vertical cylinder) around the waveguide. Thickness not in scale

Figure 5.11 shows a cross-section of the entire laminated structure obtained by an optical microscope. It is worth noting that the prepreg has slightly flowed inside the waveguide.

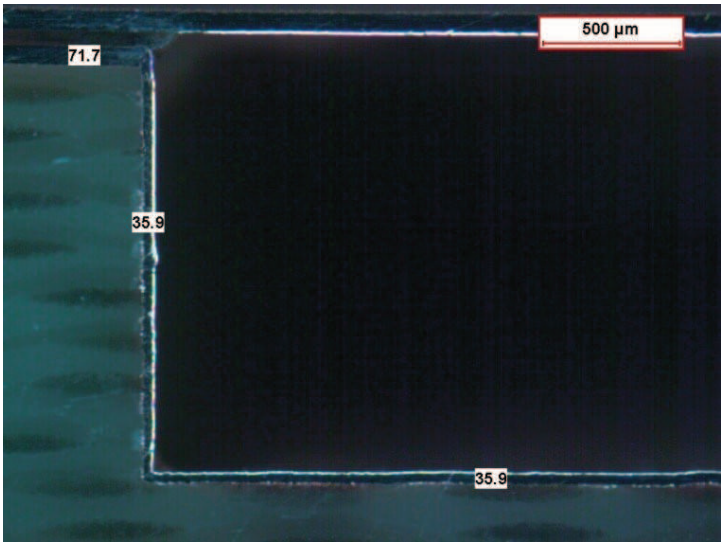


Fig. 5.11: Metallographic cross-section of the guide. The copper thickness is reported in each layer and verified the low expansion of the no-flow prepreg. It is noticeable the slight resin flow inside the guide

5.2.2. Performances

Propagative properties of the Dielectricless SIW have been compared to those of a standard waveguide. For instance, assuming perfect metal ($\sigma = \infty$), their simulated propagation constants (imaginary parts) are almost coincident (Figure 5.12). At the frequencies of interest [10.7 – 12.7] GHz, if the air gap of the Dielectricless SIW is designed with dimensions of a traditional waveguide, the error on the phase constant is less than 1%.
The structure proposed has a cutoff frequency slightly lower respect that of a traditional waveguide. This fact can be justified by the minimal part of signal that travels inside the dielectric between the two halves. As it happens for the traditional SIW, the cutoff frequencies are lower respect the equivalent DFW because a small part of the signal that spill over from the vias [22].

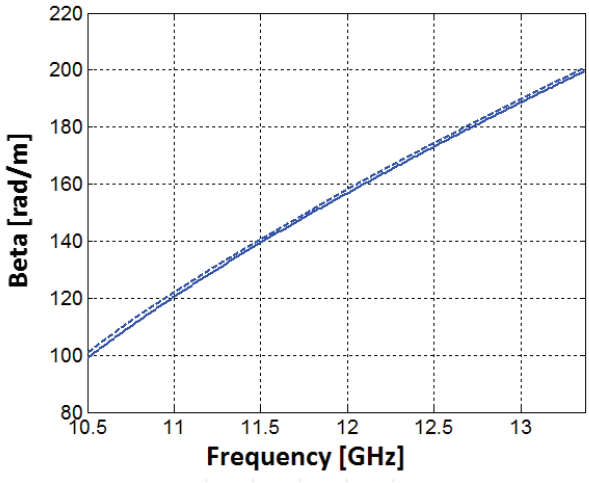


Fig. 5.12: Simulated propagation constant of the Dielectricless SIW (dashed line) and corresponding traditional waveguide (solid line), its inner dimensions are a = 16 mm and b = 1.52 mm

In order to demonstrate the advantages of such a structure in terms of losses, a comparative simulation with dielectric filled waveguides (DFW) loaded with different materials is shown in Fig. 8. As the fundamental mode TE_{10} in DFWs and SIWs is similar it is possible to use the relation (5.1) to design equivalent guides:

$$w_{eff} = \mathrm{w} - \frac{\mathrm{d}^2}{0.95\,\mathrm{s}} \qquad (5.1)$$

where w_{eff} is the equivalent width of a rectangular waveguide with the same propagative characteristics of a SIW of width w, where s is the spacing between two consecutive vias and d their diameter.
Here, the DFWs are designed to achieve the same cut-off frequency, appropriately dimensioning the width of the guides. Besides, to highlight the dielectric losses reduction which represent the dominant loss factor, perfect electric conductor (PEC) is used in all the waveguides considered in the simulations.
In this comparison typical RF material for the DFWs and low cost material for the Dielectric-Less SIW were considered, their properties being listed in Table 5.1.

Materials Involved	**D_k (ε_r)**	**D_f (tan δ)**
Taconic RF35	3.5	0.0018
Rogers RO3003	3	0.0013
Duroid 5880	2.20	0.0009
Iteq IT158	4.4	0.02
Tuc TU-84P NF	4.3	0.01
Vacuum	1	0

Tab. 5.1: Electric properties of materials used in the comparison. The two rows highlighted, are relative to the materials used in the Dielectricless SIW build-up

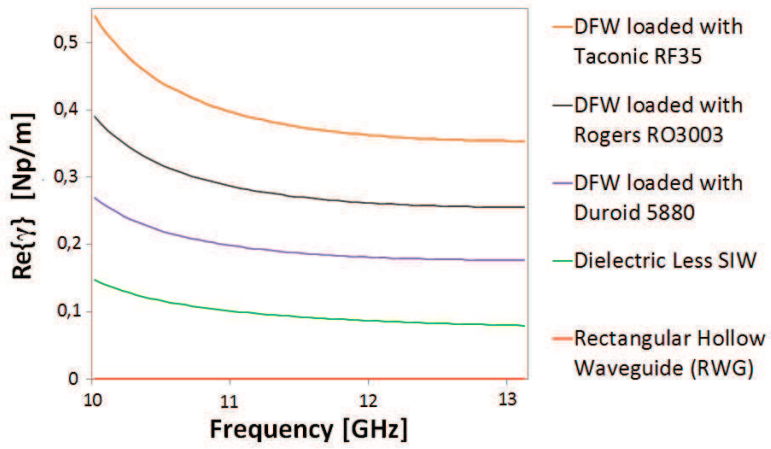


Fig. 5.13: Comparative simulation between real part of the propagation constant of waveguides filled with different materials and the proposed structure

Fig. 8 shows the attenuation (Np/m) due to different dielectrics. It is evident, that despite the use of standard low cost materials in the Dielectric-Less SIW, it is obtained a dielectric loss lower than DFWs loaded with expansive RF materials. The effective dissipation constant (tan δ) for the Dielectric-Less SIW in this simulation is about 0.0005 and it is due to the minimal portion of electromagnetic field traveling on the polymerized prepreg between the laminate with the metallized pit and the cover.

5.2.3. Slotted antenna design

As an example, a resonant slotted antenna composed of 20 slots has been designed and built. The length of each slot, 12.82 mm, has been chosen in such a way to obtain a resonating frequency of 11.75 GHz [44]. The longitudinal spacing of the slots is approximately half wavelength (in waveguide) equal to 25.64 mm, and the displacement from the center is optimized by using the Ansys High Frequency Structure Simulator electromagnetic simulator. With the same simulator, the shape of the slots has been optimized [45] in order to be easily realizable by a mechanical mill. The antenna is symmetrical with respect the middle, where is inserted the SubMiniature version A (SMA) connector. The connector, penetrating the guide, realizes a three-port junction and cannot be matched at the three ports simultaneously, as well known. Therefore, to obtain acceptable match, it was chosen to share the same reflection magnitude between all the ports; to do this, the width of the waveguide was optimized [28] to get the condition

$$|S_{11}| = |S_{22}| = |S_{33}| = 1/3 \qquad (5.2)$$

at the operating frequency. The width of the pit, allowing to satisfy the condition (5.2) is 21.5mm.
Owing to the substantial equivalence between the propagation constants in a traditional rectangular waveguide and the Dielectric-Less SIW, it has been possible to simulate the antenna, and in general other components, by approximating the Dielectric-Less SIW as a rectangular waveguide.
The width of the rectangular equivalent waveguide is set equal to the width of the milled waveguide, neglecting via holes.
The simulated geometry is shown in Figure 5.14 and a photograph of the final antenna is shown in Figure 5.15.

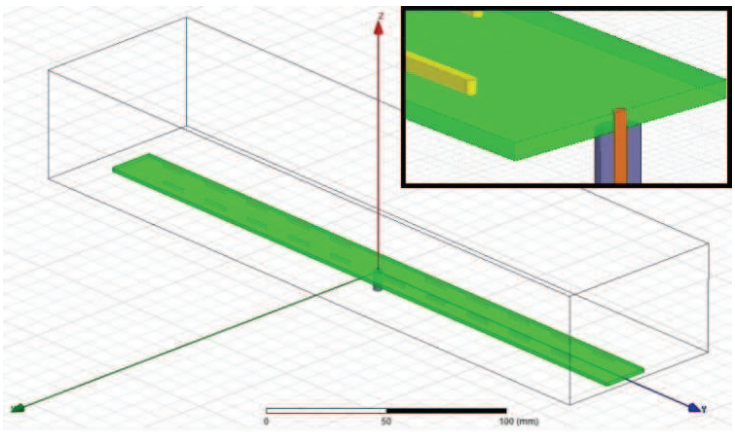


Fig. 5.14: CAD model of the designed antenna. The green box constitutes the interior part of the guide and the slots are represented on the top in yellow. It has been simulated also the SMA connector and the radiation box enclosing the structure. In detail, the cross-section of the guide in correspondence of the coaxial transition, where the purple cylinder represent the Teflon of the SMA connector and inside of it the central conductor that penetrates the Dielectric-Less waveguide

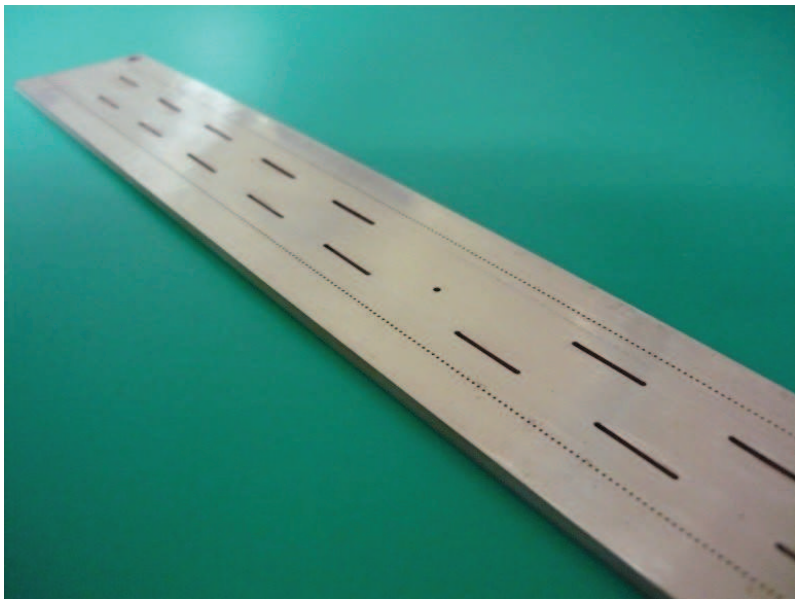


Fig. 5.15: First prototype of a dielectric-less slotted antenna. It is noticeable the series of plated through holes around the guide and the hole in the middle for the coaxial connector

The input matching and the radiation pattern have been measured and compared with the simulated results (Figures 5.16 and 5.17 respectively).

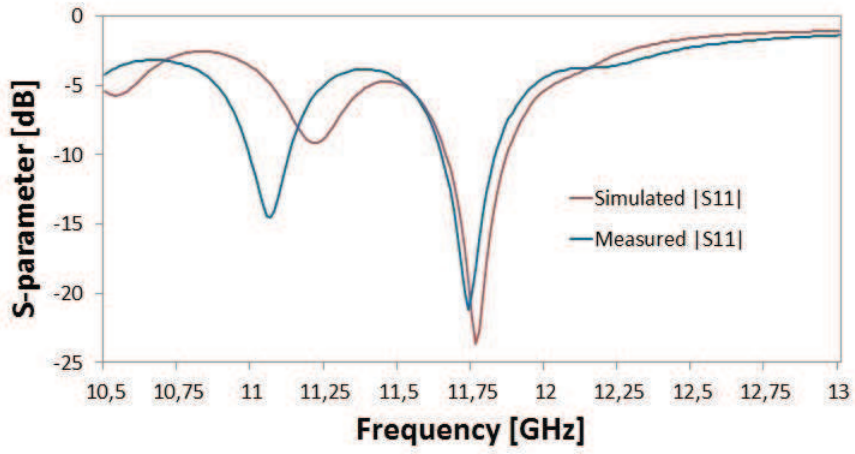


Fig. 5.16: Reflection coefficient S11 of the input port

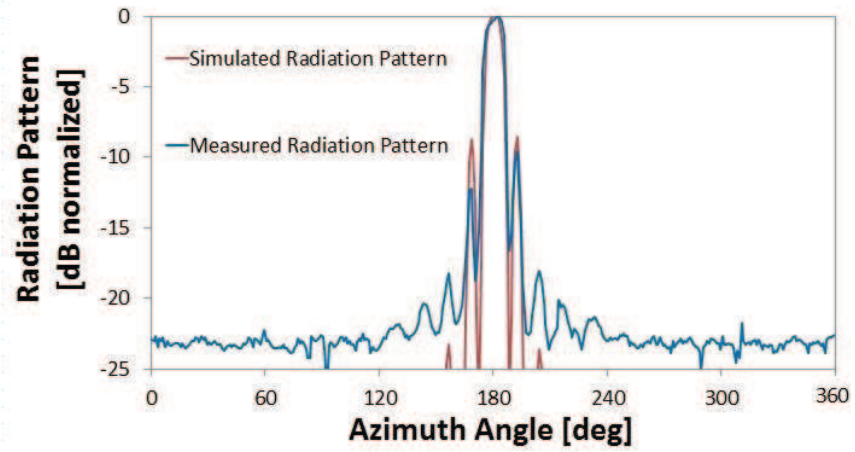


Fig. 5.17: Azimuth radiation pattern. Here, to maintain the diagram compact, simulated values inferior to -25dB were ignored because they are smaller than the sensitivity to the measuring system

As shown in the diagrams, there is a very good agreement between simulations and experimental results. A 15 dB input matching is measured over a bandwidth of 100 MHz for a relative bandwidth of 0.85%. The narrow bandwidth of this antenna is due to the length of the Dielectricless SIW cavity. The azimuthal radiation pattern is perfectly symmetrical respect to the boresight with an angular beamwidth at the half-power level (HPBW) of 8° and the distance between first nulls (FNBW) of 16°. The measured gain at 11.75 GHz is 15.45 dB versus 15.87 dB simulated, thus confirming the good correlation between a Dielectricless integrated waveguide and a traditional RWG.

5.3. Hybrid antenna development

The Dielectricless SIW configuration has proven advantages under a point of view of the losses reduction, but the removal of the dielectric has subsequences. The fact that the signal travels into the air instead of the dielectric makes the wavelength longer respect a classic SIW and subsequently also the dimensions of the components will be enlarged accordingly. Realizing a planar array like that synthetized in cfr. 4.5.4 would be impossible in Dielectricless technology because of the physical superposition of the wider elementary radiators (the distance of the slots is fixed).
Therefore, the use of the dielectric is a "must" for the elementary radiators, but at the same time it degrades the performances of signal that travels along the feed line. For the same space issues, a mixed structure SIW (radiators) – Dielectricless SIW (feed line) would not be possible over the same substrate. To sustain the same cutoff frequency for the transmission lines constituting the feed line, in fact, it would be necessary almost the double ($\sqrt{\varepsilon_r} = \sqrt{3.5} = 1.87$) of the width that again it is in contrast with the arrangement of the elementary radiators.
To maintain the dielectric in the substrate of the SIW elementary radiators and to take of the advantages of the low dissipation feed line in Dielectricless SIW, a multilayer structure has been proposed: the top laminate will host the radiators, while the bottom substrate will be machined to realize the hollow feed line (Figures 5.18 and 5.19). Then, the two substrates will be joined with prepreg, as for all the multilayer PCBs, and one aperture on each layer will be opened to realize a proper coupling between the radiators and the feed line.
Finally, the sliding of the feed line toward a different layer, releases space in the laminate with the radiators that could be realized with a different material, with less restrictions respect the Taconic RF-35A2 chosen in 4.5.

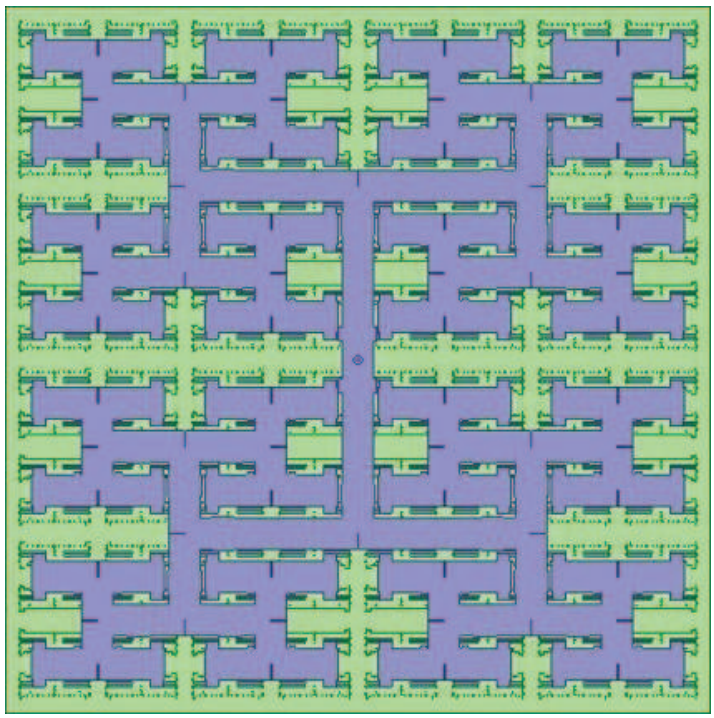


Fig. 5.18: Bottom view of the Hybrid antenna concept. On the light green laminate in background they are derived the SIW radiators. The blue draw is the corporate feed line in Dielectricless SIW technology

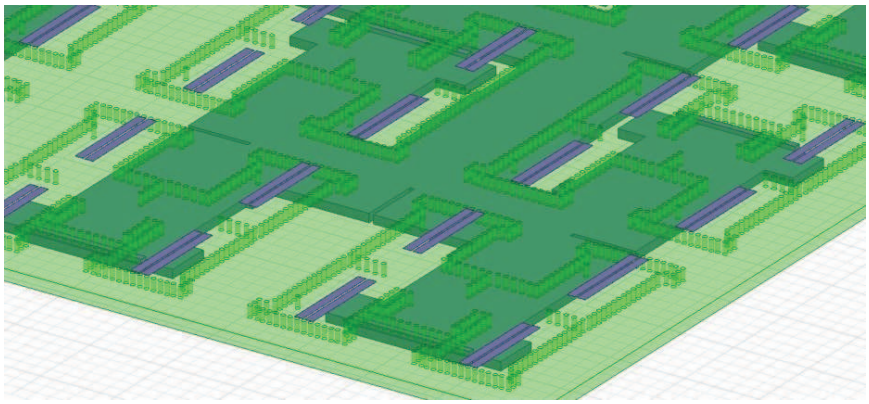


Fig. 5.19: Top-diagonal view of the Hybrid antenna. In detail the transition between the feed line and radiators

Chapter 6.

Concluding Remarks

6.1. Conclusions

In this thesis work it is summarized a significant part of the Research Project supported in part by SOMACIS S.p.A. and in part by the Italian National Project entitled "Integrated waveguides (SIW) technologies developments for ICT applications" under Grant PON01_01224/2.

The ultimate goal of the project has led the development of a class of SIW prototypes, designed by the teams of the University of Ancona and Bari, and the definition of industrial processes for their realization within the tolerances that guarantee their performance repeatability.
Substantial efforts were spent to design a low-profile (board thickness 1.52 mm) antenna array in SIW technology for receiving the DVB-S signal. Such antenna has been realized through processes normally used in the PCB industry and its gain measured over 25 dB against 29 dB expected.
To test the receiving capabilities of such antenna, a commercial LNB (Low Noise Block converted) has been connected to the array coaxial connector and the IF output of the LNB to a satellite receiver decoder. Therefore, the array was directed to satellite Eutelsat Hotbird at 13°E of longitude, with horizontal and vertical polarization alternatively. Unfortunately, due to its low gain, if compared with commercial TV dishes (more than 30 dB), only few channels have been correctly hocked.

The discrepancies between the simulated and measured antenna gain have been analyzed; in particular, the investigation lied mostly on the loss mechanism of the SIWs. As the SIW is a planar technology, it suffers from of non-idealities of the materials with which the devices are realized. The main two motives of loss are the dielectric loss, due to the lossy dielectric materials and conductor loss, due to the finite conductibility of copper. Moreover, as the SIW technology has been designed, it is present an additional loss due to the leakage between adjacent vias. The conductor loss and radiation loss can be kept reasonably contained accordingly, if some geometric parameters of the devices are controlled, conversely, dielectric losses can be reduced only using a better dielectric laminate.
A great part of this thesis focuses on the verification of material properties, in particular the dielectric constant and the loss tangent of Taconic RF-35A2 used for the all the devices here treated. Besides standard methods of measurement, a modified version of the differential phase method in SIW technology was proposed to verify the dependency of the dielectric constant on the frequency and the influence of the orientation of the waveguides compared to the bundles. This method highlighted a good consistency of dielectric constant over the

frequency and a quasi-negligible effect of the arrangement of the components compared to the fibers. Otherwise, two different methods were used to determine the dielectric loss tangent, and in both case it was found a higher value, if compared with that declared from the supplier. This could be the root cause of the difference between the simulated and measured results on the antenna gain.

In any case, the limitation on the antenna gain derives from the trade-off between the antenna directivity that increases linearly with the area of the array and the losses, mainly due to lossy dielectrics that increase exponentially with the length of the feeding network. Based on these considerations, a novel structure, here called “Dielectricless” SIW was presented. The aim of the Dielectricless SIW is to reduce strongly losses due to the dielectric, removing most of the dielectric itself from the waveguide. Components realized by this technology are lightweight, compact, low lossy and capable of handling high power. The Dielectricless SIW allows to obtain propagation characteristics comparable with the hollow rectangular waveguides, that are particularly suitable for the realization of a large and low loss feed line. With these premixes, it was proposed the concept of a hybrid multilayer structure composed of traditional SIW radiators and Dielectricless waveguide as feed line. Of course, this structure presents a higher degree of manufacturing complexity but at the same time it reduces the dielectric losses on the feed line. Furthermore, being the feed line in a separate layer compared to the radiators it allows the design of wider radiators and hence a largest choice of substrate to be used. The design presented herein could be applicable to any microwave component with same strict parameters as the high quality factor and flatness.

Another important aspect, here treated, has been the optimization of the technological aspects related to the production process derived on the use of low loss laminates. The main criticism observed has been the correct metallization, without any copper void, of through holes on PTFE substrates. Many precautions in the drilling stage had to be taken to avoid burring; this is possible only by thoroughly understanding and implementing the optimum drilling process. Moreover, all the drilling debris must be removed prior to hole wall preparation with the desmear based on plasma. To ensure a perfect metallization, and hence, to nullify the possibility of an additional loss for radiation through the hole walls, a second metallization step has been foreseen. The control tests and the verification conducted on the devices confirm the goodness of the process so defined.
These results, which comply with the specifications dictated by international standards, in the field of printed circuits, are therefore, rapidly transferable in production.

The project results can be taken as a starting point for new directions of research in the field of printed circuits boards.
The introduction of highly innovative components, with costs comparable to that realized in traditional planar technology and with significant higher performances, seems to have a promising market. It can be noticed that the conservation and the refinement of these technologies is seen in all the advanced countries as “strategic”, with a main role in the defense, surveillance and telecommunication systems.

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